# DESIGN OF A MINIATURISED ASYMMETRICAL POWER SPLITTER

# USING

# LOW IMPEDANCE ARTIFICIAL TRANSMISSION LINES

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# ABSTRACT

Transmission lines are the basic building blocks of any RF and microwave circuits. The width of a microstripline increases as the characteristic impedance is lowered for a given substrate. Wide microstriplines suffer from spurious and higher order modes at higher frequencies and may not behave as transmission lines. This means the lower limitation for a realisable microstripline is about 10 ohm. In this project microstriplines with characteristic impedances of 7 ohm and 25 ohm at a frequency of 2 GHz were designed and realised using the artificial transmission lines (ATL) concept. Detailed theoretical analysis and circuit and EM simulations were used for the design and implementation of the ATLs. Taconic TLY-5 substrate was used for the PCB fabrication. The substrate thickness was 0.787 mm and the dielectric constant was 2.2. The measured results were de-embedded and compared with the simulation results. The detailed procedure of modelling and de-embedding of an SMA connector is also given.

The 25 ohm ATL was realised using microstriplines only, where as microstriplines and chip capacitors were used in realising the 7 ohm ATL. The measured characteristic impedance of the 25 ohm ATL was 24.4 ohm and the measured electrical length of the 25 ohm ATL was 180 degrees at 2.1 GHz. To realise a 25 ohm ATL with 90 degrees electrical length, the half-wavelength 25 ohm ATL geometry was cut into half and one of the half geometries was EM simulated. The EM simulated electrical length of the 25 ohm ATL was 90 degrees at 1.9 GHz. The measured characteristic impedance of the 7 ohm ATL was 5.9 ohm and the measured electrical length of the 7 ohm ATL was 90 degrees at 1.8 GHz.

The main advantage of an ATL is size reduction. A 25 ohm meandered microstrip line (substrate thickness = 0.787 mm, dielectric constant = 2.2) with 180 degrees electrical length at 2 GHz has a size of 34 mm x 15 mm. The 25 ohm ATL with 180 degrees electrical length at 2.1 GHz was realised in a size of 22 mm x 19 mm. The design of the 25 Ω ATL resulted in 18 percent reduction in area compared to the meander line. A 7 ohm conventional microstripline (substrate thickness = 0.787 mm, dielectric constant = 2.2) with 90 degrees electrical length at 1.8 GHz has a size of about 28 mm x 27 mm. The 7 ohm ATL with 90 degrees electrical length at 1.8 GHz was realised in a size of 7 mm x 8.4 mm which is only 8 percent of the conventional 7 ohm microstripline area.

In general, a spacing of 3h where h is the substrate thickness is required between the adjacent microstriplines. In this project detailed investigations were done to see if the spacing can be reduced without any detrimental coupling affects and a spacing of 0.6 mm was used. This reduction in spacing has resulted in reduced size of the ATL.

For an asymmetrical power splitter based on the Wilkinson topology, the power splitter output power split ratio depends on the square of the characteristic impedances of the quarter-wavelength arms. In this project an asymmetrical power splitter was designed and realised using a 7 ohm ATL and a 25 ohm ATL as the quarter-wavelength arms. The desired centre frequency of the power splitter was 2 GHz and the measured centre frequency was 1.6 GHz. At the centre frequency the phase difference between the output ports of the power splitter will be zero. The simulated power split ratio was 10.1 dB and the measured power split ratio was 13 dB. The power split ratio calculated using the measured characteristic impedances of the ATLs (24.4 ohm and 5.9 ohm) will be 12.4 dB which is very close to the measured power split ratio.

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# LIST OF SYMBOLS AND ABBREVIATIONS

| Symbol | Description |
|---|---|
| $Z_o$ | characteristic impedance |
| $\varepsilon_r$ | relative dielectric constant |
| $\varepsilon_{eff}$ | effective dielectric constant |
| h | substrate thickness |
| $\lambda$ | wavelength |
| $\lambda_g$ | guide wavelength |
| $v_p$ | phase velocity |
| $C_p$ | shunt capacitance |
| d | length of a unit cell (ATL) |
| $\ell_{Stub}$ | length of the stub |
| $W_{TL}$ | microstripline width |
| $W_{Stub}$ | width of a stub |
| L | inductance per unit length |
| C | capacitance per unit length |
| $\beta$ | phase constant |
| $\Phi$ | phase of a unit cell |
| $\Phi_{ATL}$ | total phase of an ATL |
| $\sigma$ | conductance |
| $\mu$ | permeability |
| t | thickness of the copper layer |
| N | number of unit cells in an ATL |

**Abbreviations**

| | |
|---|---|
| ATL | artificial transmission line |
| MIC | microwave integrated circuit |
| MMSL | miniaturised microstripline |
| MMIC | monolithic microwave integrated circuit |
| PGB | photonic band gap |
| DGS | defective ground system |
| S-parameters | Scattering parameters |
| PCB | printed circuit board |
| CAD | computer aided design |
| CPW | coplanar wave guide |
| EM | electromagnetic |
| 3D | three dimensional |
| HEMT | high electron mobility transistor |

# CHAPTER ONE

## INTRODUCTION

Nowadays development of wireless communication systems demands more functionality in a smaller physical size. This requires complex circuit design and miniaturisation. The transmission lines i.e. microstriplines, strip lines, coplanar wave guides etc. form an integral part of the communication systems. Generally the overall size of the conventional transmission lines is large for applications in the wireless communication frequency range up to 2 GHz. So by miniaturising the transmission lines the size of the communication system can be reduced. There are many novel ways of miniaturisation of transmission lines.

Meandering of the transmission lines [1], [2] is one common way of miniaturisation. In meandering the level of miniaturisation is determined by the number of meander sections and tightness of meandering. Each meander will have four bends thus adding four discontinuities. More meander sections will result in many discontinuities. The gap between adjacent bends of the meander line can be reduced to further minimise the size but this tight meandering will result in increased parasitic coupling between transmission line sections [1]. Also the existence of sharp corners may limit the use of meandering at higher frequencies. In a meandered microstripline, the limitation of the high frequency will depend on the number of bends, bends with sharp corners and spacing between the bends.

Space-filling is another technique used for miniaturisation [3], [4]. A space-filling curve acts like a thread passing through every cell in a multi dimensional space so that every

cell visited only once; therefore the space-filling curves do not self-intersect. The space-filling curves are simple to draw and are self-similar. There are basically two types of space-filling curves i.e., closed space-filling and open space-filling. A closed space-filling curve starts and ends at the same point in a unit square, where as an open space-filling curve starts and ends at the opposite ends of a unit square. The Sierpinski fractal space-filling curve [5] is an example of closed space-filling curve as shown in Fig. 1.1 (a), and Minkowski fractal space-filling curve [6] is an example of open space-filling curve as shown in Fig. 1.1 (b). One of the main characteristics of these curves is that they can have very large perimeter while confined to a small area. The effective size reduction depends on the space-filling curve, compression ratio and the associated coupling between segments [3].

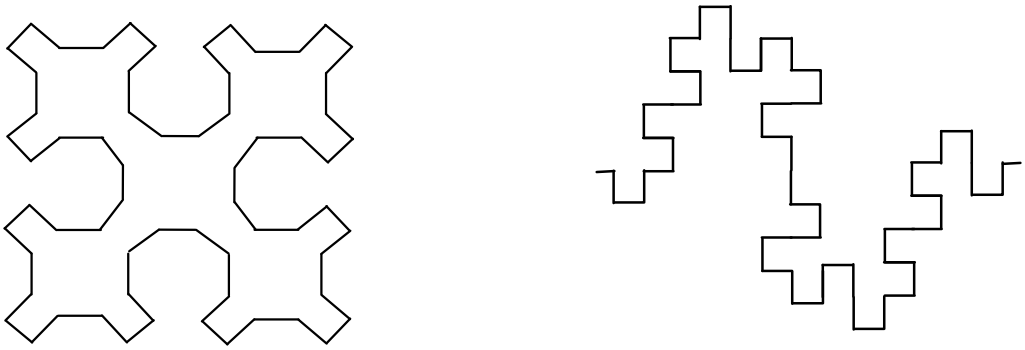



**Figure 1.1 (a) Closed space-filling curve. (b) Open space-filling curve.**

Size reduction can also be achieved by introducing capacitances at strategic points [7-9]. In a capacitively loaded Wilkinson power divider [7] as shown in Fig. 1.2, for zero reflection from all ports and infinite isolation between the output ports, the value of $C_2 = 2C_1$ and $R = 2Z_x$. The transmission line length $\ell$ is dependent on the values of $C_1$ and $Z_x$. By choosing suitable values of $C_1$ and $Z_x$, $\ell$ can be reduced. For $\ell = \lambda/10$, the required values of $Z_x$ and $C_1$ are 120 Ω and 0.12 pF at 10 GHz. The miniaturisation of the

transmission lines depend on the fabrication limitations because of the requirement of higher $Z_x$ and the availability of a low value of capacitance $C_1$. Very low capacitances can be realised by using open circuit stubs. Open circuit stubs are used in the miniaturisation of branch-line couplers [10, 11].

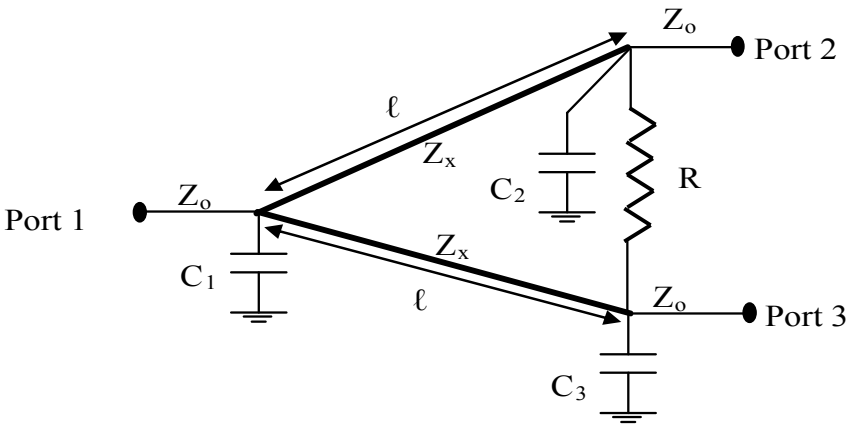



**Figure 1.2 Capacitively loaded Wilkinson power divider.**

The artificial transmission lines (ATL) concept is another method of miniaturisation [12-20]. A transmission line when periodically loaded with reactive elements can behave as a normal transmission line if the spacing between the consecutive reactive elements is much smaller than the guide wavelength. Such a periodic structure is known as an ATL. A shunt capacitance loaded ATL structure has reduced characteristic impedance and reduced phase velocity compared to a normal transmission line. The ATLs have similar behaviour in terms of phase, magnitude and characteristic impedance as normal transmission lines but smaller in size. Some of the ATL realisation methods [18-20], are more suited to monolithic microwave integrated circuits (MMICs). For example in [19], metal insulated metal (MIM) capacitors were used; in [20], ATLs were realised using miniaturised microstriplines (MMSL) comprising of air bridges and support posts. In the MMSL, the MIM capacitor effect is achieved by the support posts and the ground plane. The characteristic impedance can be increased or decreased by the

length of the support post or the width of the strip. Fig. 1.3 shows a MMSL with air bridges and support posts.

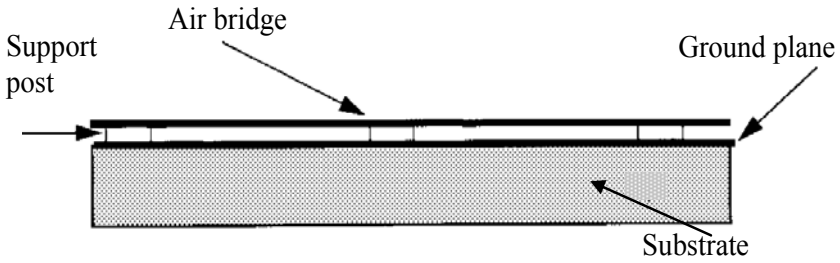



**Figure 1.3 Miniaturised microstripline.**

Power splitters are used extensively in RF/microwave amplifiers and many other test and communication equipment. Among all power dividers, the Wilkinson topology is widely used [21]. The 2-way equal power splitter is a typical application of the Wilkinson structure, because it is simple to design and easy to realise. On the contrary, realising an asymmetrical power splitter based on the Wilkinson topology is difficult due to restrictions on fabrication. For an asymmetrical power splitter based on the Wilkinson topology the ratio of the power output depends on the ratio of the characteristic impedance of the quarter-wavelength arms. For example a 1:4 Wilkinson power splitter requires one of the quarter-wave arms characteristic impedance equal to 160 Ω and the other quarter-wave arm characteristic impedance equal to 40 Ω. In practice, the maximum characteristic impedance of a realisable microstrip is limited to around 120 Ω, although it depends on the dielectric constant and the thickness of the substrate. So realising a 160 Ω transmission line using conventional microstrip structure is impractical. The 1:4 Wilkinson power splitter can also be realised by using a 100 Ω and a 25 Ω quarter-wave arms. The minimum characteristic impedance of a realisable microstripline is limited to around 40 Ω and realising a 25 Ω transmission line using conventional microstrip structure is difficult.

To overcome the limitations in realising the higher characteristic impedance, novel design methods have to be used to increase the characteristic impedance of the microstripline for a given width, so that it can be fabricated. Different methods have been used in realising the asymmetrical power splitter [22-27] based on the Wilkinson power splitter with one of the arms using high impedance quarter-wave transmission line. In [22], the high impedance quarter-wave transmission line of the asymmetrical power splitter was realised using lumped elements. In [23-25], the high impedance transmission line was realised by adopting a defective ground system (DGS). In a DGS the microstripline has etched defects in the ground plane. The advantage of using the DGS under the microstripline is that the characteristic impedance of the microstripline increases due to the effective inductance generated by the DGS. By using this method, microstriplines with characteristic impedances around 200 Ω were achieved.

An asymmetrical power splitter can also be realised using the low impedance transmission line as one of the quarter-wave arms. So far very limited research was done in realising a very low impedance transmission line. In [20], a low impedance coplanar wave guide was realised using MMSL, which is very difficult to fabricate because of the air bridges and support posts.

In this thesis, a miniaturised asymmetrical power splitter was realised using low impedance transmission lines. The low impedance transmission lines were realised using the ATL concept. The low impedance transmission lines also find applications in high current laser diodes [28] and in matching networks where low impedance devices such as power FETs [29], high electron mobility transistors (HEMT), pseudomorphic HEMT's (pHEMT) or photodiodes are used.

## 1.1 Thesis Structure

In this project the ATL concept is used for miniaturisation. The theory of the ATL and the involved design equations are presented in Chapter 2. AWR Microwave Office was used for the circuit and EM simulation. Chapter 3 discusses the software used.

In this project, the transmission lines with characteristic impedances of 25 Ω and 7 Ω were realised using the ATL concept. Chapters 4 and 5 of this thesis discuss the design and realisation of the 25 Ω and 7 Ω ATLs respectively. Using these two ATLs an asymmetrical power splitter was realised based on the Wilkinson power splitter. The asymmetrical power splitter is a three-port network with unequal power outputs but with no phase difference between the two output ports. All the three port impedances were 50 Ω. Chapter 6 of this thesis discusses the realisation of the asymmetrical power splitter that uses the 25 Ω and 7 Ω ATLs. The conclusions of this thesis are given in Chapter 7.

Standard PCB technology was used for fabricating the ATLs and the asymmetric power splitter, because they were constructed entirely using microstriplines and lumped elements. Taconic TLY-5 substrate with thickness of 0.787 mm and dielectric constant ($\varepsilon_r$) of 2.2 was used in this project. The data sheet of the substrate material is attached in Appendix 1. Surface mount chip capacitors were used in realising the 7 Ω ATL; the data sheet of the chip capacitor is attached in Appendix 2. The circuit and EM simulations and experimental results were used to confirm the design approach for the ATLs and the asymmetrical power splitter.

# CHAPTER TWO

## THEORY OF ARTIFICIAL TRANSMISSION LINES

### 2.1 Theory

A transmission line or a wave-guide periodically loaded with reactive elements is referred to as a periodic structure [30]. Fig. 2.1 shows a periodic structure comprising a transmission line periodically loaded with shunt capacitances $C_p$. The transmission line is characterised by its characteristic impedance $Z_{oTL}$ and its phase velocity $v_{pTL.}$ A periodic structure shown in Fig. 2.1 can be visualised as a number of unit cells connected in cascade. The unit cell is defined as one period of the structure.

A periodic structure behaves as a normal transmission line when the unit cell length $d$ is sufficiently small (less than $0.1\lambda_g$) compared to the guide wavelength. Such a periodic structure is known as an artificial transmission line (ATL) [12]. The ATL shown in Fig. 2.1 has reduced characteristic impedance and phase velocity compared to $Z_{oTL}$ and $v_{pTL}$. Reduced phase velocity means an ATL as shown in Fig. 2.1 can be shorter than a conventional transmission line for the same electrical length.

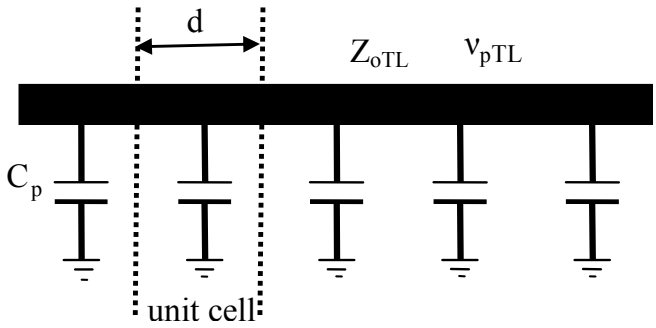



**Figure 2.1 A periodic structure.**

## 2.2 ABCD matrix of a of Short Length Transmission Line

Fig. 2.2 shows a lossless transmission line of length *d*.

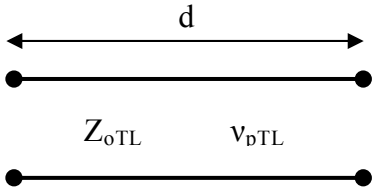



**Figure 2.2 Short length of a transmission line.**

The transmission line is described by its characteristic impedance $Z_{oTL}$ and its phase velocity $v_{pTL}$. The characteristic impedance and phase velocity are related to the distributed inductance *L* (H/m), and distributed capacitance *C* (F/m):

$$Z_{oTL} = \sqrt{\frac{L}{C}} \tag{1}$$

$$v_{pTL} = \frac{1}{\sqrt{LC}}. \tag{2}$$

The distributed parameters, *L* and *C* can be obtained by solving equations (1) and (2):

$$L = \frac{Z_{oTL}}{v_{pTL}} \tag{3}$$

$$C = \frac{1}{Z_{oTL} v_{pTL}}. \tag{4}$$

The ABCD matrix of a transmission line of arbitrary length is [31] :

$$\text{ABCD}_{\text{TL}} = \begin{bmatrix} \cos(\beta_{TL} d) & jZ_o \sin(\beta_{TL} d) \\ \dfrac{j \sin(\beta_{TL} d)}{Z_{oTL}} & \cos(\beta_{TL} d) \end{bmatrix} \tag{5}$$

where

$$\beta_{TL} = \frac{\omega}{v_{pTL}}, \tag{6}$$

and $\omega$ is the angular frequency equal to $2\pi f$. When $d$ is much smaller than the wavelength ($d << \lambda$), $\beta_{TL} d << 1$, and hence:

$$\cos(\beta_{TL} d) \approx 1 - \frac{(\beta_{TL} d)^2}{2}, \tag{7}$$

$$\sin(\beta_{TL} d) \approx \beta_{TL} d \, . \tag{8}$$

Substituting (7) and (8) in (5), the ABCD matrix of a short length of transmission line is:

$$\text{ABCD}_{\text{TL}} \approx \begin{bmatrix} 1 - \frac{(\beta_{TL} d)^2}{2} & j Z_o \beta_{TL} d \\ j \frac{\beta_{TL} d}{Z_o} & 1 - \frac{(\beta_{TL} d)^2}{2} \end{bmatrix}. \tag{9}$$

Using equations (1), (2) and (6):

$$\text{ABCD}_{\text{TL}} \approx \begin{bmatrix} 1 - \frac{(\omega d)^2 (LC)}{2} & j\omega L d \\ j\omega C d & 1 - \frac{(\omega d)^2 (LC)}{2} \end{bmatrix}. \tag{10}$$

Fig. 2.3 shows a lowpass LC T-network.

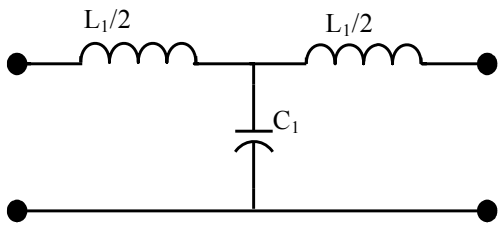



**Figure 2.3 Lumped element equivalent of a short length transmission line.**

The ABCD matrix of the lowpass filter shown in Fig. 2.3 can be written as [31]:

$$\mathrm{ABCD_{LC}} = \begin{bmatrix} 1-\dfrac{\omega^2(L_1C_1)}{2} & j\omega L_1 \\ j\omega C_1 & 1-\dfrac{\omega^2(L_1C_1)}{2} \end{bmatrix}. \tag{11}$$

Comparing the ABCD matrix of the lowpass LC network (11) with the ABCD matrix of the short length of transmission line (10), it can be seen that they have same functional behaviour with respect to $\omega$, and are identical if:

$$L_1 = Ld \tag{12}$$

$$C_1 = Cd. \tag{13}$$

The conclusion is that a short length of transmission line can be modelled as a lowpass LC network as shown in Fig. 2.3 or alternatively, a lowpass LC network shown in Fig. 2.3 can be modelled as a short length of a transmission line. This result is used in the analysis of an ATL.

## 2.3 Characteristic impedance and phase velocity of an ATL

Fig. 2.4 shows a unit cell of an ATL comprising of a short length of a transmission line of length $d$ ($d < 0.1\ \lambda_g$) loaded by a shunt capacitance $C_p$.

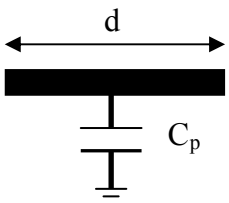



**Figure 2.4 A unit cell of an ATL.**

In section 2.2 it was shown that a short length of a transmission line can be modelled as a lowpass LC network and $L_1 = Ld$, $C_1 = Cd$. Using these findings a unit cell can be modelled as shown in Fig. 2.5.

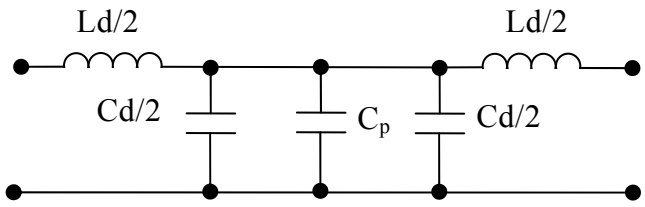



**Figure 2.5 Equivalent circuit of a unit cell.**

Comparing Fig. 2.3 with Fig. 2.5,

$$L_1 = Ld \quad \text{and} \quad C_1 = Cd + C_p. \tag{14}$$

From (14), the effective distributed parameters of an ATL comprised of unit cells shown in Fig. 2.5 are:

$$L_1/d = L \tag{15}$$

$$C_1/d = C + C_p/d. \tag{16}$$

Using (2), the phase velocity of an ATL,

$$v_{pATL} = \frac{1}{\sqrt{L\left(C + \frac{C_p}{d}\right)}}. \tag{17}$$

The characteristic impedance of the ATL, $Z_{oATL}$ can be obtained by substituting the values $L_1/d$ and $C_1/d$ from (15) and (16) respectively in (1),

$$Z_{oATL} = \sqrt{\frac{L}{C + \frac{C_p}{d}}}. \tag{18}$$

From (17) and (18), it can be noted that the phase velocity and the characteristic impedance reduce with increasing the shunt capacitance.

## 2.4 Design equations for the ATL

An artificial transmission line structure with *N* unit cells is shown in Fig. 2.6. Each unit cell is of length *d* ($d << \lambda_g$) and has a shunt capacitance $C_p$.

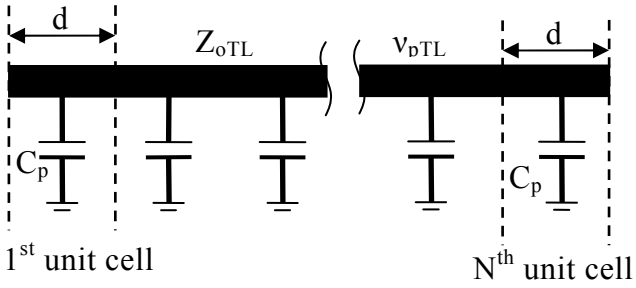



**Figure 2.6 An ATL structure with N unit cells.**

The electrical length [12] of the ATL structure shown in Fig. 2.6 is:

$$\Phi_{ATL} = dN\beta_{ATL} \tag{19}$$

where *N* is number of unit cells and

$$\beta_{ATL} = \frac{\omega}{v_{pATL}}. \tag{20}$$

Substituting (20) in (19), the electrical length of the ATL is [12]:

$$\Phi_{ATL} = dN\omega\sqrt{L\left(C + \frac{C_p}{d}\right)}\ . \tag{21}$$

Rearranging (18):

$$\sqrt{L\left(C+\frac{C_p}{d}\right)}=\frac{L}{Z_{oATL}}. \tag{22}$$

Substituting (22) in (21) and rearranging:

$$d=\frac{Z_{oATL}\Phi_{ATL}}{\omega LN}. \tag{23}$$

Substituting the value of $L$ from (3) in (23), the equation for $d$, can be written as [12]:

$$d=\frac{Z_{oATL}\Phi_{ATL}v_{pTL}}{\omega Z_{oTL}N}. \tag{24}$$

From equation (18) the lumped capacitance $C_p$ is:

$$C_p=\left(\frac{L}{Z_{oATL}^2}-C\right)d. \tag{25}$$

Substituting the value of $d$ from (24) in (25),

$$C_p=\left(\frac{L}{Z_{oATL}^2}-C\right)\left(\frac{Z_{oATL}\Phi_{ATL}v_{pTL}}{\omega Z_{oTL}N}\right). \tag{26}$$

Substituting the values of $L$ and $C$ from (3) and (4) in (26) and rearranging:

$$C_p=\frac{\Phi_{ATL}(Z_{oTL}^2-Z_{oATL}^2)}{N\omega Z_{oTL}^2 Z_{oATL}}. \tag{27}$$

For a given transmission line ($Z_{oTL}$, $v_{pTL}$) and required values of $Z_{oATL}$ and $\Phi_{ATL}$, the value of shunt capacitance $C_p$ can be found by using (27) [12].

Open circuit stubs may be used in place of shunt capacitances. Fig. 2.7 shows an ATL with shunt open circuit stubs.

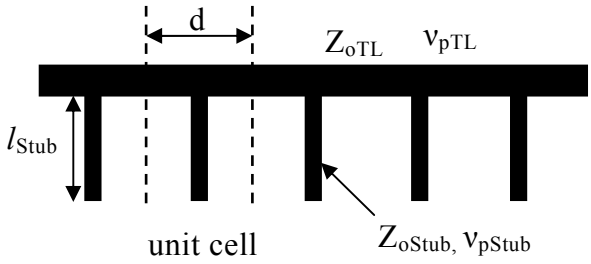



**Figure 2.7 An ATL with shunt stubs.**

The input admittance of an open circuit stub is:

$$Y_{Stub} = \frac{j\tan(\beta_{Stub} l_{Stub})}{Z_{oStub}} \tag{28}$$

where $\beta_{Stub} = \frac{\omega}{v_{pStub}}$.

The admittance of a capacitor is $j\omega C_p$ and the input admittance of the open circuit stub needs to be equal to the capacitor admittance. Therefore [12] :

$$j\omega C_p = \frac{j\tan(\beta_{Stub} l_{Stub})}{Z_{oStub}}. \tag{29}$$

Rearranging (29):

$$l_{Stub} = \frac{1}{\beta_{Stub}} \tan^{-1}(\omega Z_{oStub} C_p), \tag{30}$$

where stub length $l_{Stub}$ has to be much smaller than the guide wavelength ($l_{Stub} << \lambda_g/10$).

The choice of $Z_{oTL}$ and $Z_{oStub}$ determine the width of the main transmission line and the stub respectively. The characteristic impedances are related to the width of the microstrip [31] :

$$Z_o = \begin{cases} \dfrac{60}{\sqrt{\varepsilon_{eff}}} \ln\left(\dfrac{8h}{W} + \dfrac{W}{4h}\right) & \text{for} \quad \dfrac{W}{h} \le 1 \\ \dfrac{120\pi}{\sqrt{\varepsilon_{eff}}\left[\dfrac{W}{h} + 1.393 + 0.667 \ln\left(\dfrac{W}{h} + 1.444\right)\right]} & \text{for} \quad \dfrac{W}{h} \ge 1 \end{cases} . \tag{31}$$

The phase velocity of a microstrip is related to an effective dielectric constant $\varepsilon_{eff}$ :

$$v_p = \frac{c}{\sqrt{\varepsilon_{eff}}} \tag{32}$$

where [31]:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(\frac{1}{\sqrt{1 + 12h/W}}\right). \tag{33}$$

In this chapter, the theory of the ATL and the various design equations required to realise the ATL were shown. These design equations were used in designing the ATLs and the design and realisation of the ATLs is explained in Chapters 4 and 5.

# CHAPTER THREE

## CAD TOOLS USED

Applied Wave Research's Microwave Office (MWO) [1] 2004, version 6.5 was used for the circuit and the EM simulations. A substrate (TYL-5 Taconic) with dielectric constant $\varepsilon_r$ = 2.2 and thickness h =0.787 mm was used in this project. As per the data sheet attached in Appendix 1, the dielectric loss tangent (tan δ) at 2 GHz is 0.005. The detailed description of the circuit simulation is given in section 3.1 and the description of the EM simulation is given in section 3.2.

### 3.1 Circuit simulation

A schematic is a graphical representation of a circuit. Schematics were created using a database of lumped elements, microstriplines, transmission lines, substrates, sources and ports etc. In this project the ATLs were realised using microstriplines and the chip capacitors. When microstriplines are used in the circuit simulation, the substrate details have to be defined in the schematic.

Microwave Office database contains microstrip elements such as lines (microstriplines, traces, open and short circuited stubs etc.), junctions (T-junctions, crosses) and bends. These elements are useful in simulating a circuit layout. The microstrip elements can be circuit models or EM models. The circuit model consists of formulas describing the

[1] Microwave Office 2004, AWR corp. http://web.awrcorp.com/

electrical properties of the element. The EM discontinuity models use the results of the full-wave EM solutions of the discontinuity to more accurately model the discontinuity as a parameterised circuit element.

In Microwave Office circuit simulator, sub-circuits can be added to the schematics. A sub-circuit is a circuit block that can be a schematic, a net list, an EM structure or a data file. To add a data file as a sub-circuit, the data file needs to be imported. In this project EM structures and data files were used as sub-circuits.

In schematics the parameters can be made as variables. The variables can be tuned using a real-time tuner to see the effects on the responses or can be optimised setting optimisation goals. This feature of tuning and optimisation was used in this project.

## 3.2 EM simulation

The circuit simulator does not take into account of parasitic coupling effects between the transmission lines. To account for parasitic coupling, an electromagnetic (EM) simulator was used. The EM simulator uses Maxwell's equations to compute the response of a structure from its physical geometry. EM simulators can simulate highly arbitrary structures. In addition, EM simulators are not subject to many of the constraints of the circuit models because they use fundamental equations to compute the response. EMSight is the EM simulator in Microwave Office. EMSight is a full-wave EM solver based on a modified spectral-domain method of moments (MoM) [32]. The spectral-domain method of moments has been widely used for microstriplines and other planar structures [33]. This method is used to accurately determine the

multi-port scattering parameters for passive planar structures. The planar structures include vias, vertical metal sheets and any number of layers of metal traces embedded in a stratified dielectric substrate. The planar structures are predominantly made of microstriplines, striplines, coplanar waveguides and PCBs (single and multiple layers). As the current project is based on microstrip structures, spectral-domain method of moments is more suitable for the EM simulations. However EMSight cannot be used for solving 3D arbitrary structures (require volume mesh technique) such as structures with slant boundaries and curved surfaces.

The planar structure to be analysed is placed in a metal enclosure. The enclosure defines the boundary conditions, the dielectric materials for each of the layers and the cell size. In EMSight, the boundary conditions for the sidewalls of the enclosure are always perfect conductors and cannot be modified. The top and bottom boundaries are by default perfect conductors and can be modified as per the application. In this project perfect conductors were used for top and bottom boundaries.

EMSight requires at least two dielectric layers to be defined. In this project microstrip structures were simulated and modelled with two dielectric layers: the top dielectric was air and the lower dielectric was the substrate with $\varepsilon_r$ of 2.2 and tan $\delta$ of 0.005. The separation between the EM structure and the top boundary was kept more than $\lambda_g/10$. Fig. 3.1 illustrates the dialog box used for setting up the dielectric layers in EMSight. In the dielectric layers setup, the thickness, the dielectric constant and the loss tangent of the dielectric are mentioned. In Fig. 3.1, layer 2 defines the substrate used in the simulation; thickness = 0.787 mm, $\varepsilon_r$ = 2.2 and tan $\delta$ = 0.005. For multilayered circuits,

the layers can be added by using the “add above’ and “add below” menu controls. Each layer can be coloured differently for better visibility and easy identification.

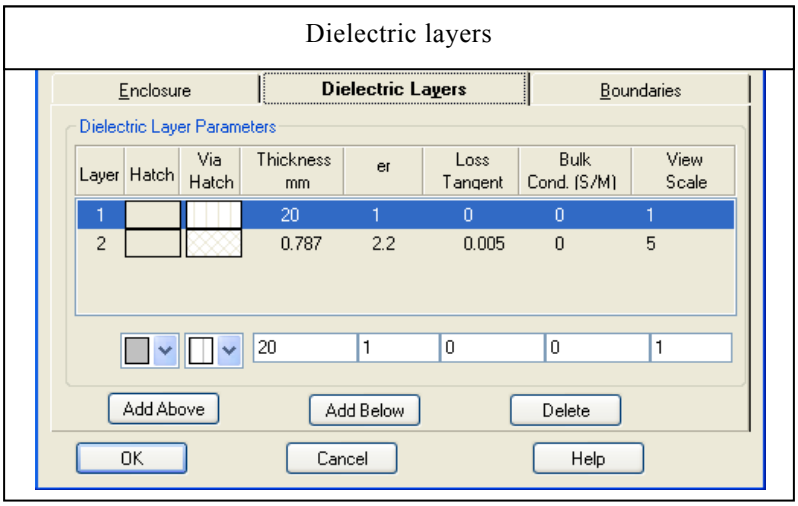



**Figure 3.1 Dielectric layers setup in EMSight.**

EMSight automatically generates gridded and variable cell size mesh which places smaller cells in areas that have high variations in current densities and large cells in areas with less current variation. Most circuits require a cell size smaller than 1/100 of the wavelength of the highest frequency of analysis. The cell size also depends on the dimension of the structure and the complexity of the structure. A large cell size results in unacceptable errors due to the incorrect modelling of the distributed effects across the cell. Although a small cell results in more accurate calculations, it also results in a longer computation time and more memory is required. The cell size also sets the geometric resolution. A cell size of 0.1 mm x 0.1 mm allows one to define the geometric features down to 0.1 mm. In this project, a cell size of 0.1 mm by 0.1 mm was used wherever possible. Figure 3.2 illustrates the dialog box used for setting up the cell size and the enclosure dimensions in EMSight.

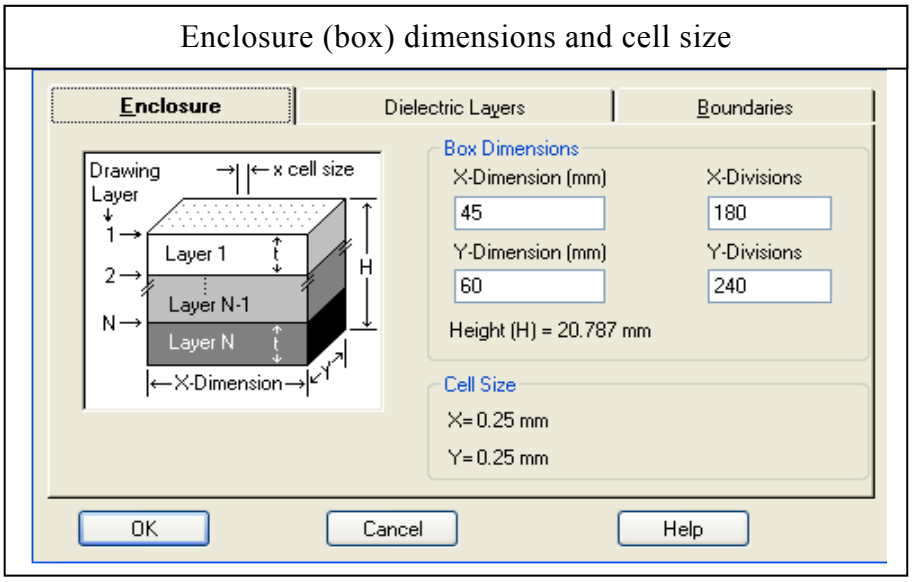



**Figure 3.2 Enclosure dimensions and cell size setup in EMSight.**

A box defines the boundaries on four sides of the circuit substrate. The box size depends on the size of the structure to be simulated. The X and Y –axis dimensions in Fig. 3.2 are the box dimensions (length and the width). The H dimension includes the substrate thickness and the air above the substrate. The box (metal enclosure) behaves as a rectangular cavity and will resonate when the length of the box equals to the half guide wavelength or the multiples of half guide wavelength. The box resonance can have a significant effect on the S-parameters in a small band centred around the resonance frequency. The best way to avoid the box resonance is to decrease the box dimensions so that the resonant frequency falls out of the wanted frequency band.

EMSight supports different types of ports. Edge ports and internal ports were used in this project. To avoid coupling, a gap of more than three times the substrate thickness is left between the EM structure and the sidewalls of the enclosure. If the side walls are too close to the circuit then the circuit's fringing fields may interact with the side walls.

The length of line from the enclosure sidewalls (port) to the reference planes is called a feedline. EMSight performs automatic de-embedding to find out the S-parameters of the EM structure using the reference planes. De-embedding removes the effects of the port discontinuities and the feedlines from the results of the simulation. Fig. 3.3 illustrates the edge ports, the feedlines and the reference planes; the feedlines have a thick black line indicating the length to be removed in the de-embedding process.

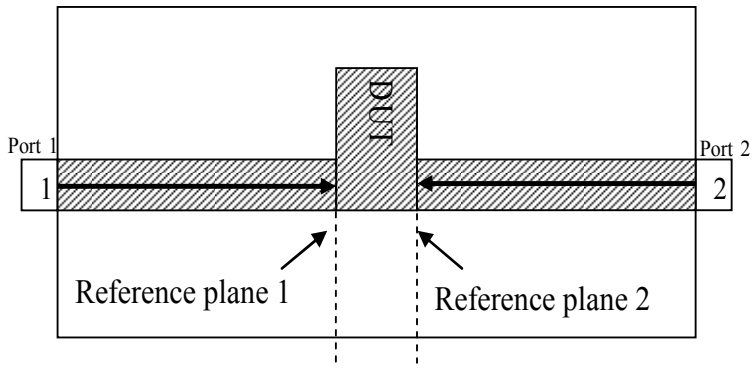



**Figure 3.3 Edge ports, feedlines and reference planes.**

# CHAPTER FOUR

## 25 Ω ARTIFICIAL TRANSMISSION LINE

### 4.1 Introduction

A 25 Ω microstripline with 180° electrical length at 2 GHz will be 6.1 mm wide and 53 mm long if laid on a 0.787 mm thick substrate with a dielectric constant of 2.2. Such a wide and long microstrip will consume lot of PCB area. Meandering could be used for miniaturisation but as explained in Chapter 1, it would reduce the bandwidth due to bends [1], and tight meandering may result in increased parasitic coupling. To achieve compact size compared to a meandered structure, the ATL concept [12-20] was used to realise a 25 Ω transmission line with an electrical length of 180° at 2 GHz. A 0.787 mm thick Taconic TLY-5 substrate with a dielectric constant of 2.2 was used for the ATL fabrication.

An ATL can be constructed as shown in Fig. 4.1 using the design equations derived in Chapter 2.

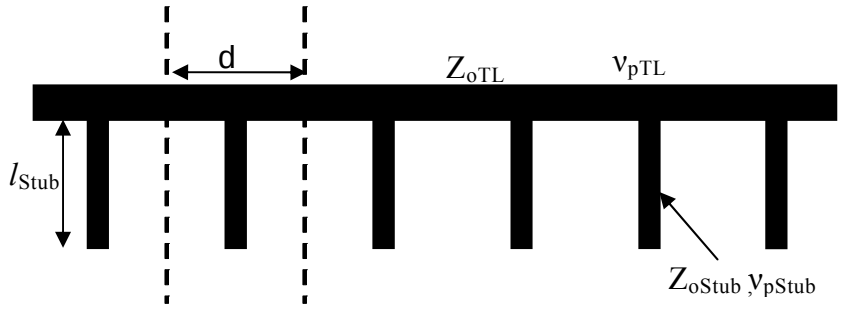



**Figure 4.1 An ATL structure.**

As a compact structure is desired, meandering and space-filling techniques were used to achieve a smaller structure as shown in Fig. 4.2. In the right hand illustration in

Fig. 4.2, the open circuited stubs facing each other may have some interaction because of the fringe fields.

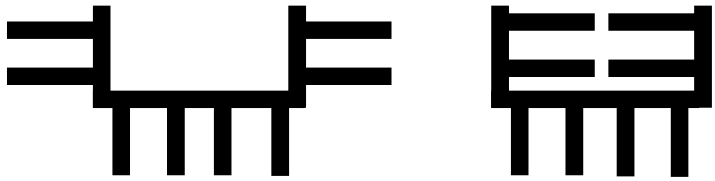


**Figure 4.2 Meandering and space-filling for further size reduction.**

In general a spacing of 3*h* [34], where h is the thickness of the substrate, is required between adjacent microstriplines to avoid any parasitic coupling between them. In Fig. 4.2, it can be seen that the size of the structure can be reduced if the spacing between the stubs is reduced. In this project a detailed study has been carried out to see the effect of placing the stubs closer (spacing less than 3*h*) and the details of the experiment and the results are given in section 4.2. The parametric analysis was carried out to find out the most suitable parameters for realising the 25 Ω ATL and the details of the analysis is given in section 4.3. The circuit and EM simulation setup and the results are given in sections 4.4 and 4.5 respectively. Details of the ATL characterisation is given in section 4.6. The experiment description and the test fixture modelling and optimisation for the de-embedding process are given in sections 4.7 and 4.8. The 25 Ω ATL raw measured data and the de-embedded measured data are given in section 4.9 and the size comparison of the ATL with a meandered 25 Ω microstripline is given in section 4.10.

## 4.2 Stub spacing

If a substrate of 0.787 mm thickness is used then the recommended spacing between adjacent stubs is 2.4 mm, and if there are large numbers of stubs used then the stubs

will occupy large amount of space. To find out the minimum space required between adjacent stubs without any parasitic coupling effects, EM simulations were carried out for the stubs placed with different spacing between them. In this particular analysis, several 12 mm long (about 0.1 $\lambda_g$ at 2 GHz), 1 mm wide open circuit stubs with spacing between them varied from 0.6 mm to 2.4 mm were EM simulated. The input admittances of the individual stubs were plotted against the frequency.

The input admittance of an open circuit stub:

$$Y_{in} = \frac{j \tan(\beta l)}{Z_o}, \tag{34}$$

where $$\beta = \frac{2\pi}{\lambda_g} \quad (\lambda_g \text{ is the guide wavelength}) \tag{35}$$

and $$\lambda_g = \frac{c}{f\sqrt{\varepsilon_{eff}}}, \tag{36}$$

$\varepsilon_{eff}$ is the effective dielectric constant calculated using equation (33).

For a 1 mm wide microstrip on a substrate with $\varepsilon_r$ of 2.2, thickness of 0.787 mm and at 2 GHz, the guide wavelength $(\lambda_g)$ can be calculated using equation (36) and is equal to 112.1 mm. Using (31), the characteristic impedance $Z_o$ is equal to 83.7 Ω. Substituting the values of $Z_o$ and $\lambda_g$ in (34) the input admittance $Y_{in}$ for a 12 mm ($\lambda_g$/10) long and 1 mm wide open circuit microstrip stub at 2 GHz is j9.55 mS.

Fig. 4.3 shows the setup for the EM simulation of eight open circuit stubs. The box and the cell size are shown in Fig. 4.3.

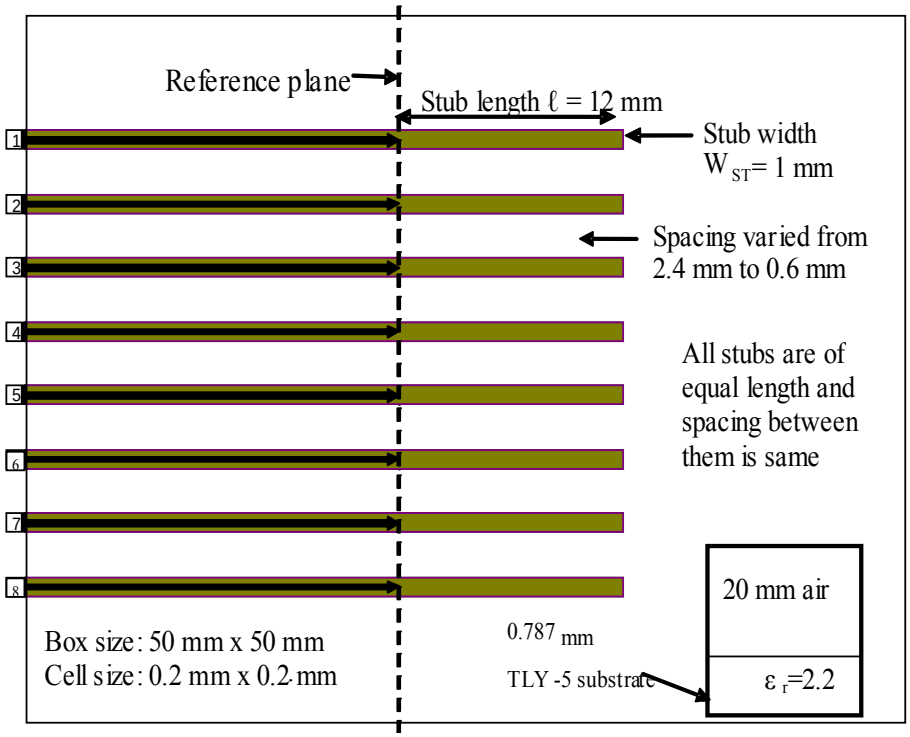



**Figure 4.3 EM simulation setup for the 12 mm stubs with variable spacing.**

The EM simulation results are shown in Fig. 4.4 to 4.6.

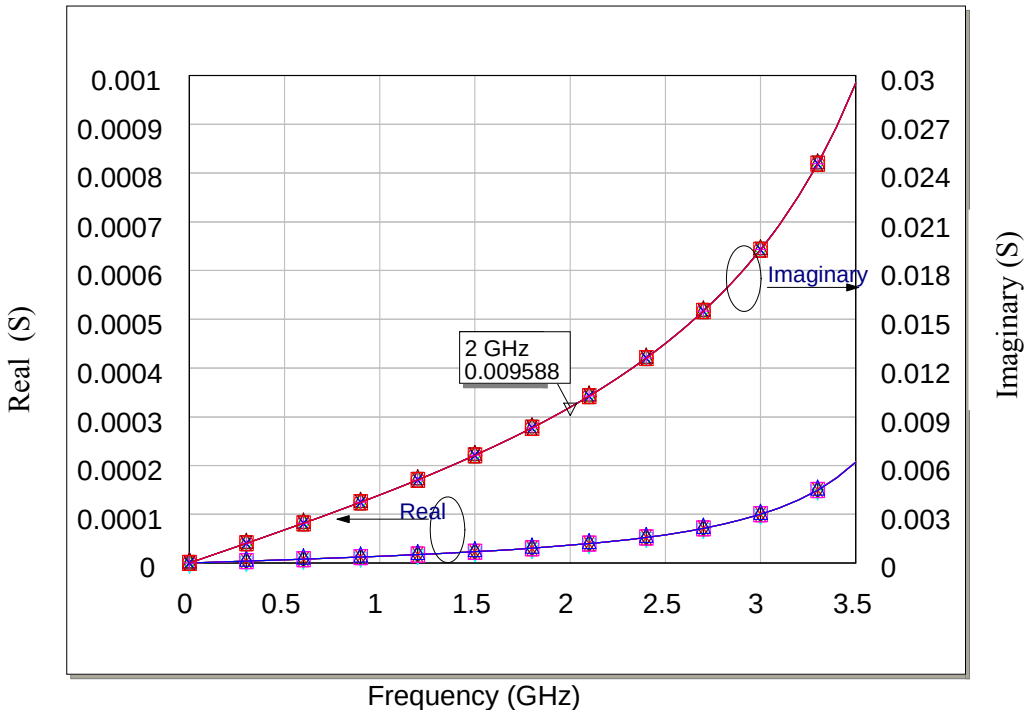



**Figure 4.4 Input admittances of 12 mm stubs with 2.4 mm spacing.**

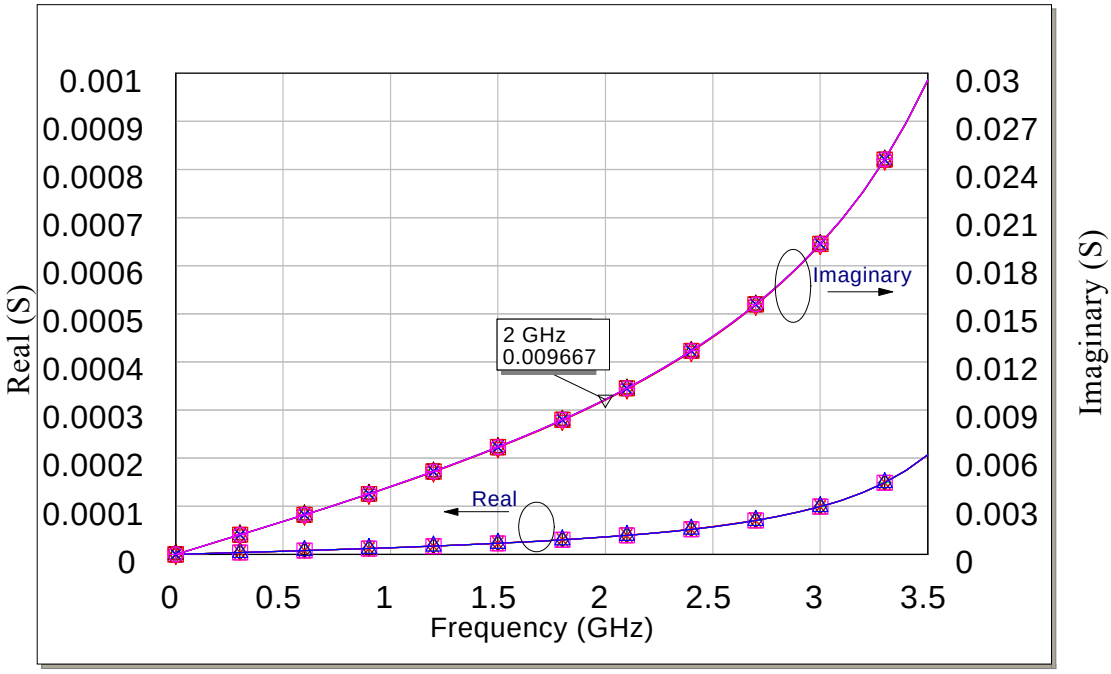



**Figure 4.5 Input admittances of 12 mm stubs with 1.2 mm spacing.**

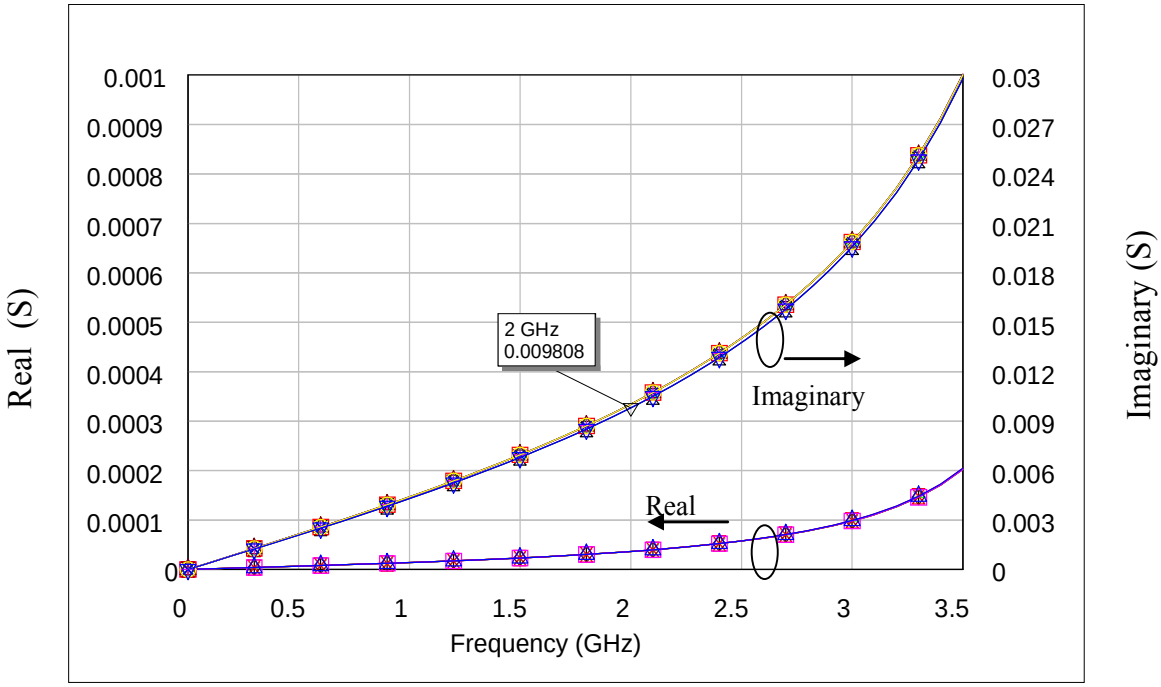



**Figure 4.6 Input admittances of 12 mm stubs with 0.6 mm spacing.**

It can be seen from the graphs shown in Fig. 4.4 to Fig. 4.6 that the input admittance of the 12 mm stub is in the range of 9.5 mS to 9.8 mS at 2 GHz as calculated using (34). It

can be seen from Fig. 4.4 to Fig. 4.6 that the input admittance of all the stubs is same irrespective of the position of the stub, indicating that there is no coupling between the stubs. The results show that the spacing rule [34] of $3h$ between adjacent stubs may not be hard and fast. It can be concluded that the stubs can be placed as close as 0.6 mm without any detrimental coupling effects.

## 4.3 Parametric analysis

The parametric analysis was carried out to find out the most suitable parameters i.e. the width of the transmission line ($W_{TL}$), the stub length ($\ell_{Stub}$), the stub width ($W_{Stub}$), and the unit cell length ($d$) for realising the 25 Ω ATL.

In Chapter 2, relationships between the parameters of an ATL - namely $W_{TL,}$ $\ell_{Stub}$, $W_{Stub}$ and $d$ were developed. In this section, the relationship between the parameters of the ATL was analysed with imposed constraints such as minimum width of the microstripline of 0.5 mm (fabrication limitation) and maximum length of the stub $0.1\lambda_{g.}$ The parametric analysis was based on $\Phi_{ATL}$= 180° at $f$ = 2 GHz, $Z_{oATL}$ = 25 Ω, $h$ = 0.787 mm, and $\varepsilon_r$ = 2.2. Detailed description of the analysis and results are presented in the following sections.

### 4.3.1 Relation between ATL length and $W_{TL}$

If there are $N$ unit cells in an ATL, then the total length of the ATL is $Nd$. The equation (24) can be rearranged as:

$$\text{ATL length} = Nd = \frac{Z_{oATL}\Phi_{ATL}v_{pTL}}{\omega Z_{oTL}}, \tag{37}$$

where the various parameter are defined in Fig. 4.7. Given $W_{TL}$, the characteristic impedance of the microstripline $Z_{oTL}$ can be calculated using (31), and $\nu_{pTL}$ can be calculated using (32). Using (37), the relation between the ATL length and $W_{TL}$ is shown in Fig. 4.8. It is clear from Fig. 4.8 that, if $W_{TL}$ is reduced, then the ATL length decreases.

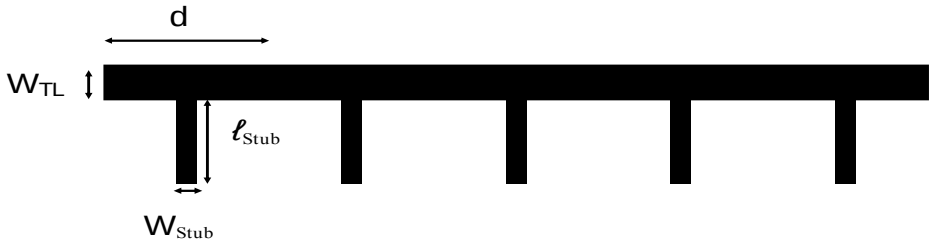



**Figure 4.7 An artificial transmission line structure.**

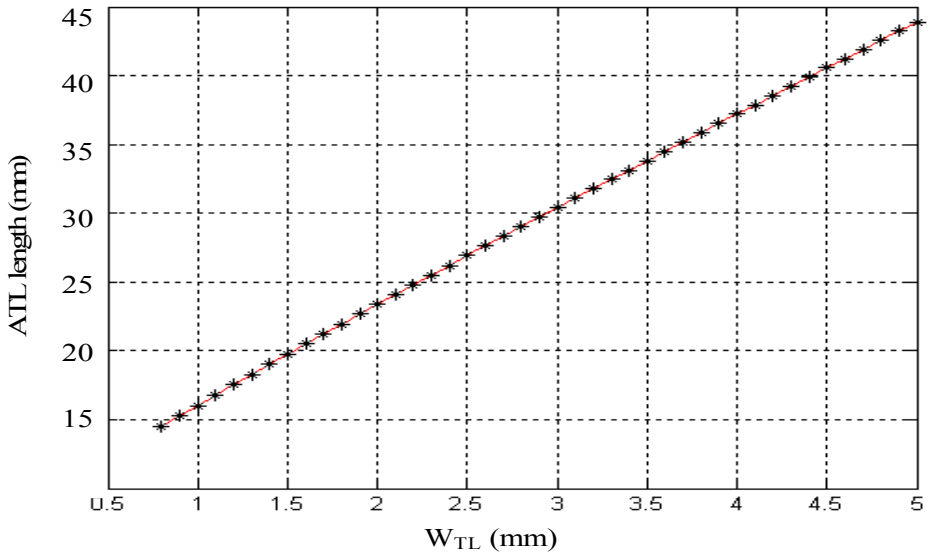



**Figure 4.8 Plot of the ATL length versus $W_{TL}$.**

### 4.3.2 Relation between $C_p$ and $W_{TL}$

Using (27) the relationship between $C_p$ and $W_{TL}$ for various values of $N$ is shown in Fig. 4.9.

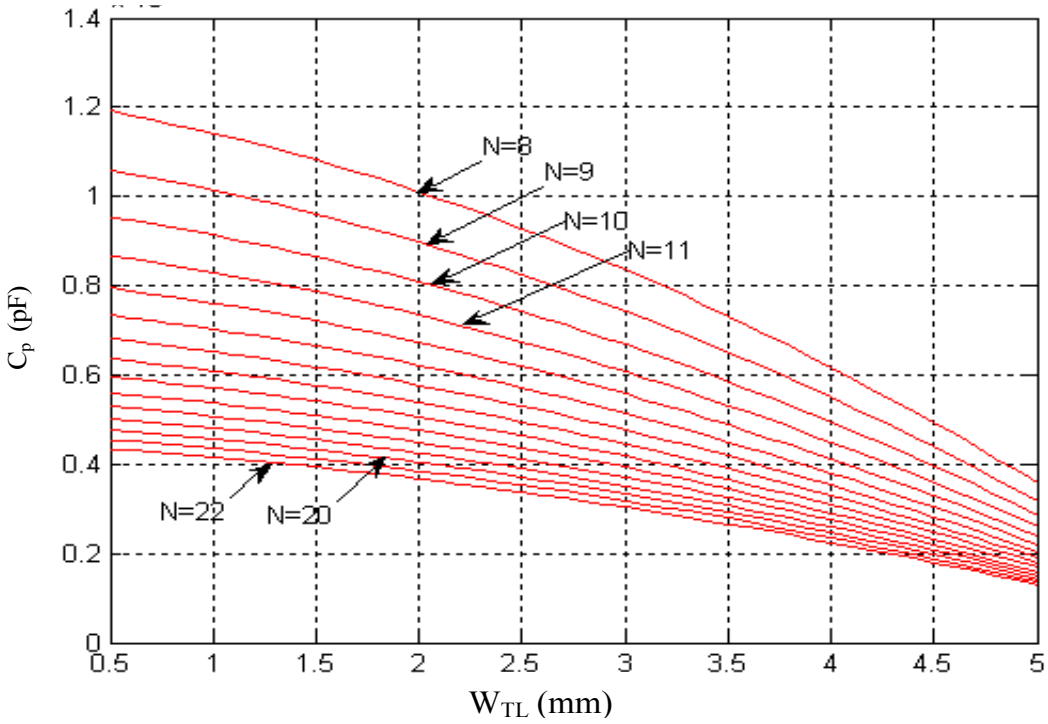



**Figure 4.9 Plot of $C_p$ versus $W_{TL}$.**

It can be seen in Fig. 4.9 that, increasing the width of the microstripline reduces the capacitance required, which means short stubs can be used. It can also be seen that larger the value of $N$ smaller the $C_p$. The variation in $C_p$ is very small for $N$ = 20 and above. So $N$ = 20 was chosen for further parametric analysis.

### 4.3.3 Relation between $\ell_{Stub}$ and $W_{Stub}$

Using (30), the relationship between $\ell_{Stub}$ and $W_{Stub}$ for various values of $W_{TL}$ and $N$ fixed at 20 is shown in Fig. 4.10. Equation (31) was used to obtain $Z_{oStub}$ from $W_{Stub}$.

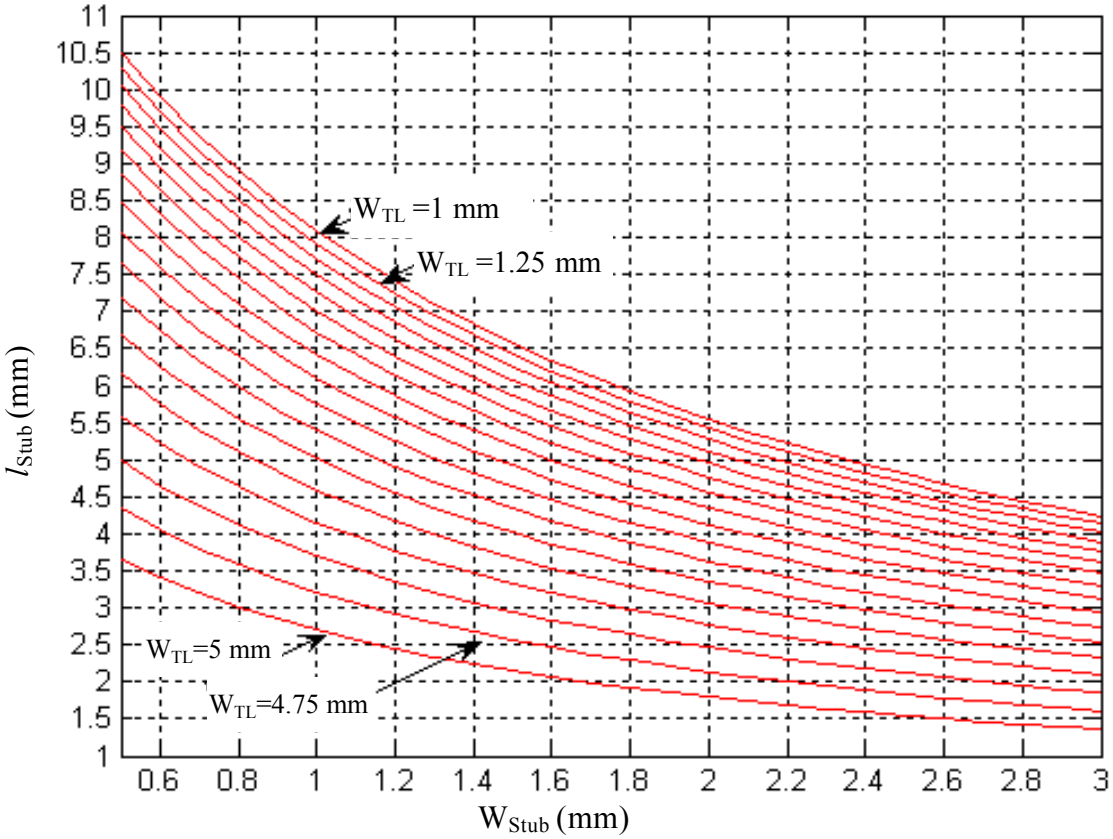



**Figure 4.10 Plot of $\ell_{Stub}$ versus $W_{Stub}$.**

It can be noticed in Fig. 4.10 that the maximum $\ell_{Stub}$ value plotted is smaller than 11.2 mm (0.1 λg) and that means all the stub lengths in the graph can be considered for realising the 25 Ω ATL. From Fig. 4.10 it is evident that an ATL with similar characteristics can have short stub lengths if wide stubs are used. But the stub width has to be smaller than *d*.

### 4.3.4 Final parameter values

With reference to Fig. 4.8, a small value of $W_{TL}$ is required for a short ATL. If $W_{TL}$ of 1 mm is chosen then the ATL length will be 17 mm. Fig. 4.10 confirms that $W_{TL}$ of 1 mm satisfies a stub length, $\ell_{Stub}$, of less than 0.1λg. But for a compact structure the stubs should be as short as possible. From Fig. 4.10, it can be seen that short stub

lengths require wide stubs; Fig. 4.11 illustrates this. Also if *s* is the minimum spacing between two stubs then *d* will be dependent on the stub width. So wide stubs mean that *d* will be large and so the ATL length will increase.

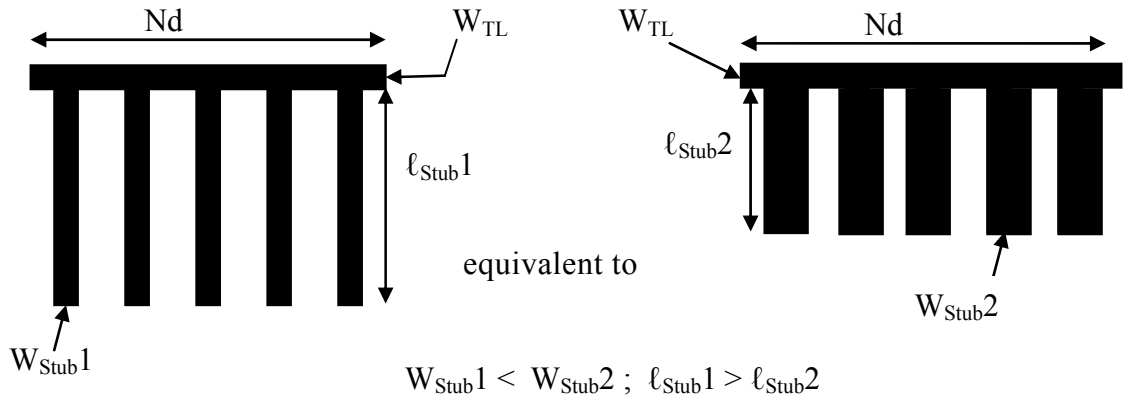



**Figure 4.11 Illustration of the relation between width and length of the stub.**

Using the graphical analysis explained above, the following parameter values were chosen for realising the 25 Ω ATL. $W_{Stub}$ = 1 mm and $N$ = 20. With a minimum stub spacing, $s$, of 0.6 mm, the minimum unit cell length, $d$, will be 1.6 mm and the ATL length $Nd$ will be 32 mm. From Fig. 4.8, it can be seen that for an ATL length of 32 mm, $W_{TL}$ is 3.3 mm. To confirm the values obtained from graphs, numerical calculations were done using the equations derived in Chapter 2. These calculations were performed with $W_{TL}$ = 3.3 mm and $N$ = 20. For an ATL with characteristic impedance $Z_{oATL}$ of 25 Ω and phase length $\Phi_{ATL}$ of 180º at 2 GHz, $d$ can be calculated using equation (24). For a microstrip of $W_{TL}$ = 3.3 mm, $Z_{oTL}$ equals to 40.1 Ω (using (31)). The Phase velocity $v_{pTL}$ was calculated using equation (32), with the effective dielectric constant calculated using equation (33).

Substituting the values of $Z_{oATL}$, $\Phi_{ATL}$, $N$, $Z_{oTL}$, $\omega$, and $v_{pTL}$ in equation (24),

$$d = 1.68 \text{ mm}.$$

Similarly $C_p$ was calculated using equation (27) and $C_p$ = 0.305 pF. The capacitance $C_p$ was realised using an open circuit stub. For $W_{Stub}$ = 1 mm, using equation (31), $Z_{oStub}$ = 83.5 Ω. The length of the stub was calculated using equation (30) and $\ell_{Stub}$ =5.6 mm.

The final values used for realising the 25 Ω ATL are tabulated in table 4.1.

| Parameter | Value |
|---|---|
| $W_{TL}$ | 3.3 mm |
| $N$ | 20 |
| $W_{Stub}$ | 1 mm |
| $C_p$ | 0.305 pF |
| $d$ | 1.68 mm |
| $\ell_{Stub}$ | 5.6 mm |

**Table 4.1 Parameter values for the 25 Ω ATL.**

## 4.4 Circuit simulation of the 25 Ω ATL

Fig. 4.12 shows the schematic of the 25 Ω ATL based upon the parameters given in table 4.1. The ATL consists of 25 unit cells ($N$=25); the first and the last elements are microstriplines with length $d/2$ and width 3.3 mm. The schematic is based on Fig. 2.6.

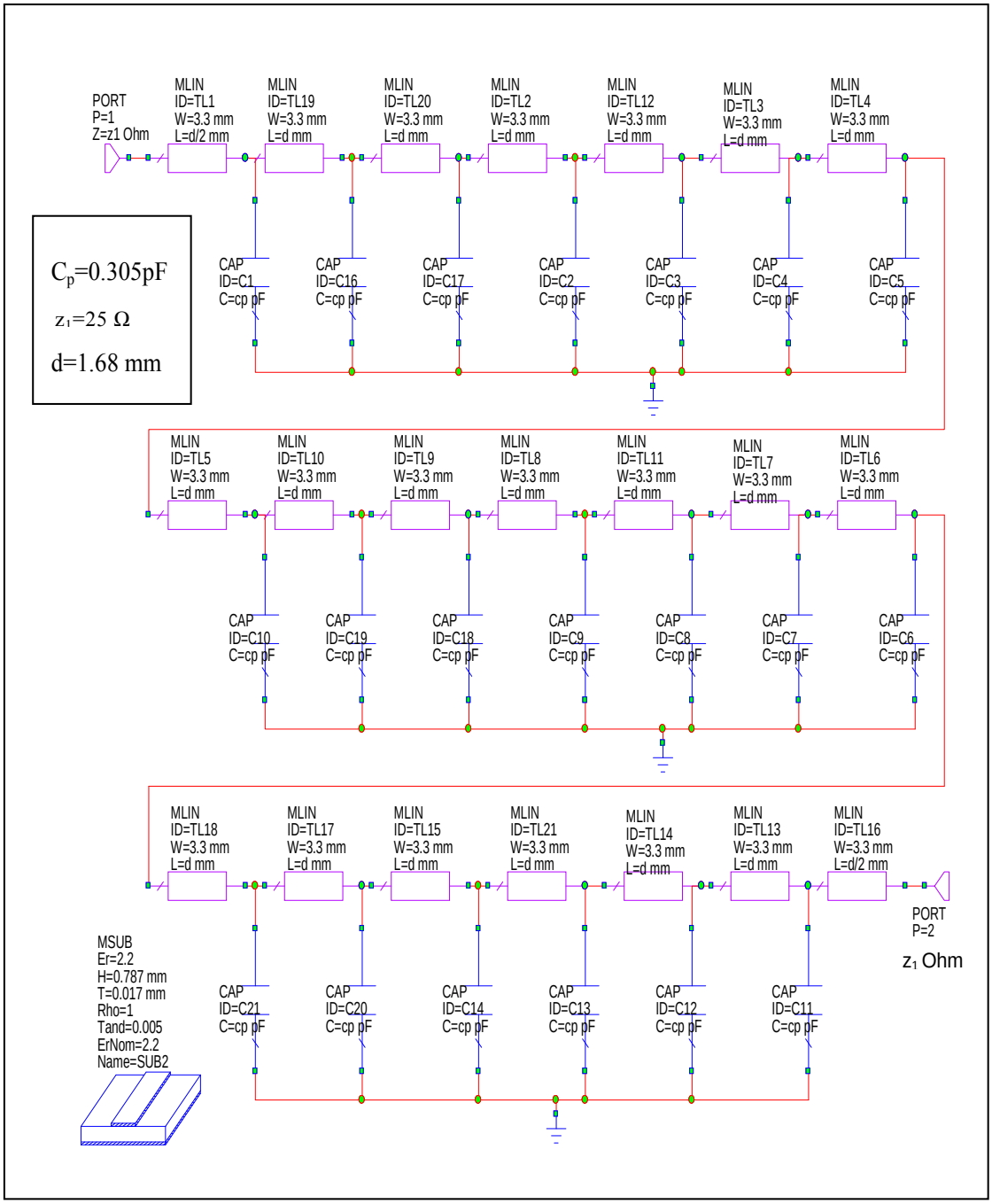



**Figure 4.12 Schematic of the 25 Ω ATL with shunt capacitors.**

The capacitors are placed at the centre of the unit cells. The input and output ports are with impedance $z_1$, where the $z_1$ is set to 25 Ω. The substrate details for the microstriplines are provided in the schematic. First circuit simulation was carried out

with lumped capacitors ($C_p$). The S-parameter simulation results with the port reference impedance equal to 25 Ω are shown in Fig. 4.13.

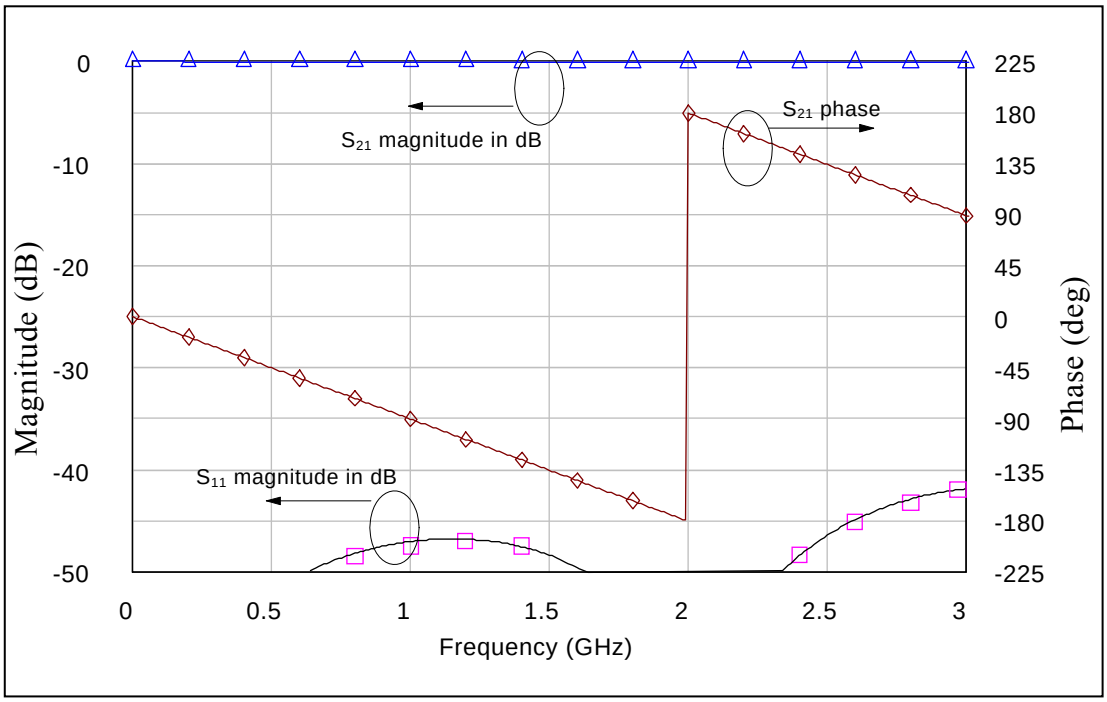



**Figure 4.13 Circuit simulated S-parameter responses of the 25 Ω ATL with shunt capacitors (Port reference impedance = 25 Ω).**

The magnitude response of $S_{22}$ is not shown in Fig. 4.13 and it will be same as the magnitude response of $S_{11}$ because the circuit is symmetric. The $S_{11}$ magnitude response in Fig. 4.13 indicates that the characteristic impedance is close to 25 Ω. The $S_{21}$ phase response shows that the phase of the ATL is 180° at 2 GHz as required.

Fig. 4.14 shows the schematic of the 25 Ω ATL with shunt capacitances replaced with shunt open circuit stubs. Fig. 4.15 shows the S-parameter simulation results with the port reference impedance equal to 25 Ω.

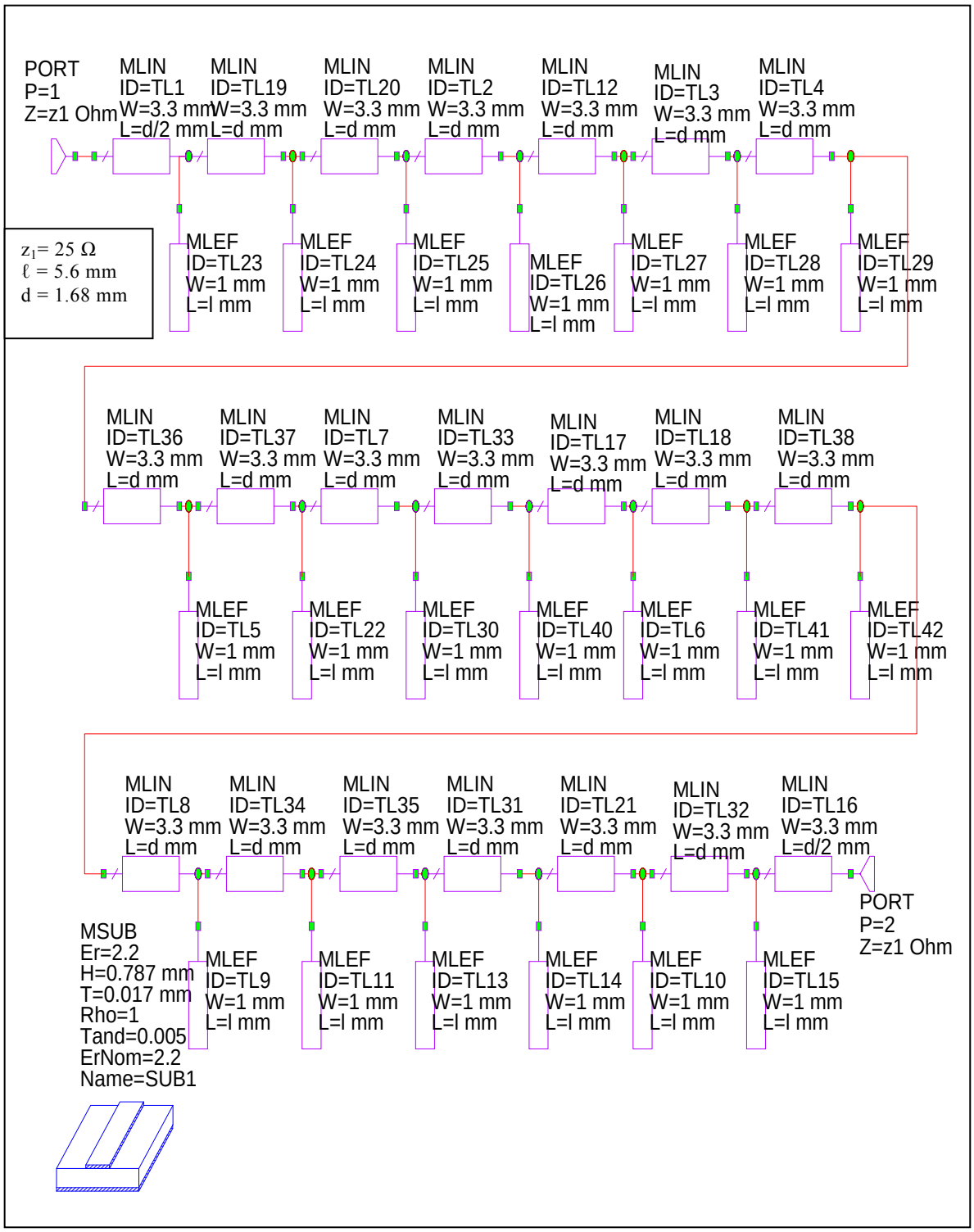



**Figure 4.14 Schematic of the 25 Ω ATL with shunt stubs.**

Fig. 4.15 also shows the S-parameter responses of the 25 Ω ATL with the shunt capacitances for comparison purposes. The S-parameter responses with the shunt capacitors are better than the S-parameter responses with the shunt stubs because the later suffers from the discontinuities arising due the T-junctions (microstripline and the stub junction). The magnitude response of the $S_{11}$ for the ATL with the shunt stubs is better than -30 dB up to 2.6 GHz, indicating that the shunt stubs can be used for realising an ATL. Also the magnitude responses of $S_{21}$ are acceptable for the ATL with the shunt stubs.

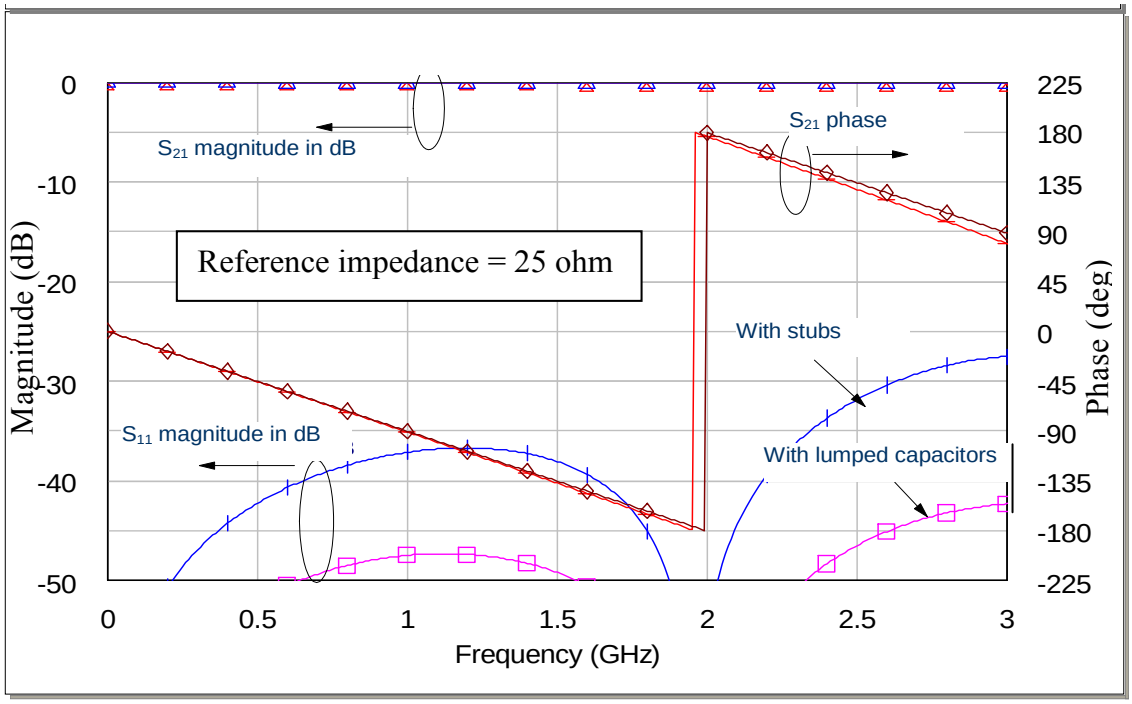



**Figure 4.15 Comparison of the circuit simulated S-parameter responses of the 25 Ω ATL with shunt capacitors and shunt stubs (Port reference impedance = 25 Ω).**

The $S_{11}$ magnitude responses in Fig. 4.15 indicate that the characteristic impedance of the ATL is close to 25 Ω. Also it can be seen from the $S_{21}$ phase response that the phase of the ATL is 180° at 2 GHz as required. The circuit simulation of the 25 Ω ATL will not take into account of the coupling effects between the microstriplines. To account

for the parasitic coupling, the EM simulation of the 25 Ω ATL is required; section 4.5 describes the EM simulation of the 25 Ω ATL.

## 4.5 EM Simulation of the 25 Ω ATL

The ATL geometry as shown in Fig. 4.1 will occupy lot of space. To save space and to achieve a compact structure, the main microstripline was meandered and stubs were placed facing each other. Final ATL structure is shown in Fig. 4.16.

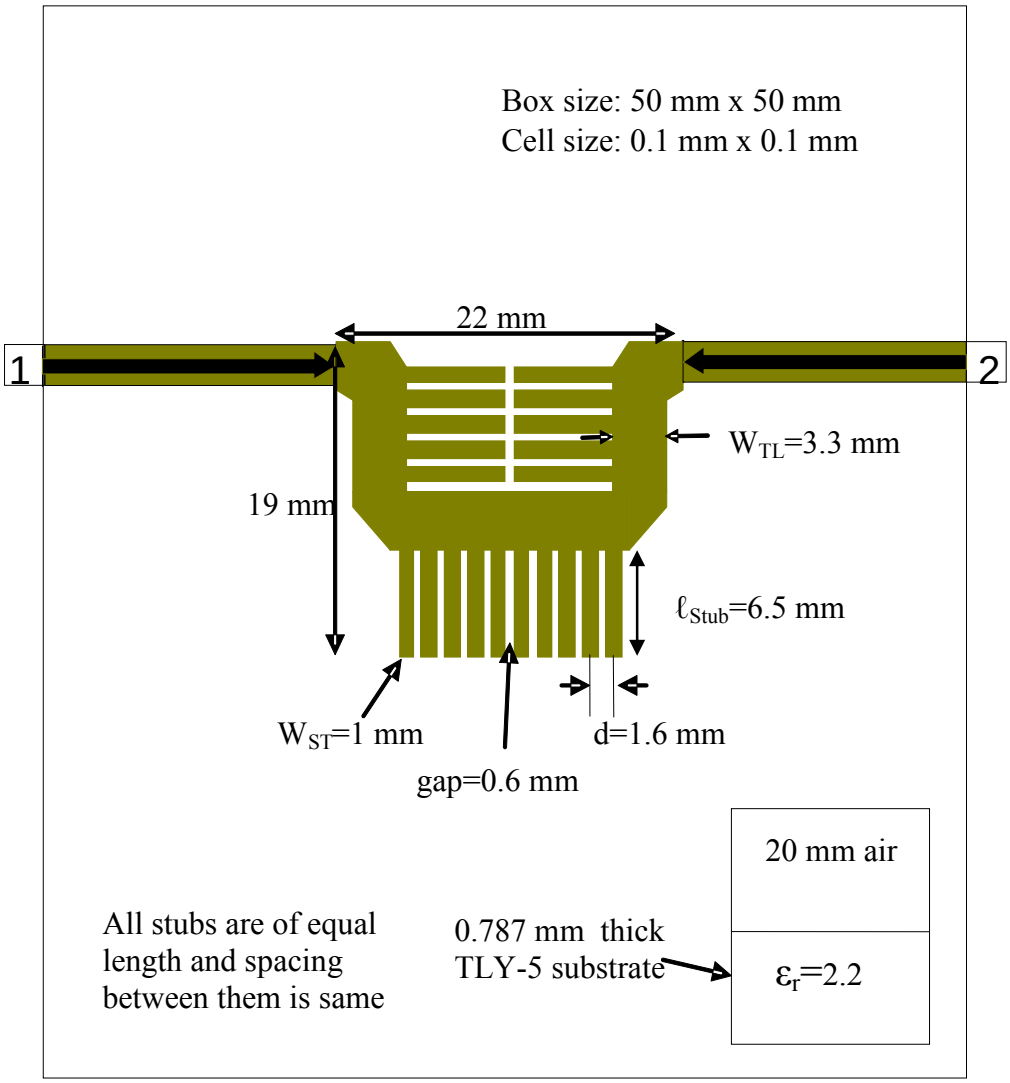



**Figure 4.16 EM simulation setup for the 25 Ω ATL structure.**

For the EM simulation the box size and the cell size are shown in Fig. 4.16. Initially the EM simulation was carried out with the stub length of 5.6 mm. To find out the characteristic impedance of the structure, port impedances were made as variable and tuned for minimum returnloss. The EM simulation S-parameter responses of the ATL structure showed that the electrical length of the ATL was 180° at 2.4 GHz. To achieve the electrical length of 180° at 2 GHz, the stub length was increased to 6.5 mm and the structure was EM simulated. The S-parameter responses with the tuned port reference impedance of 24.9 Ω are shown in Fig. 4.17; as the ATL structure is symmetric, only $S_{11}$ and $S_{21}$ responses are shown.

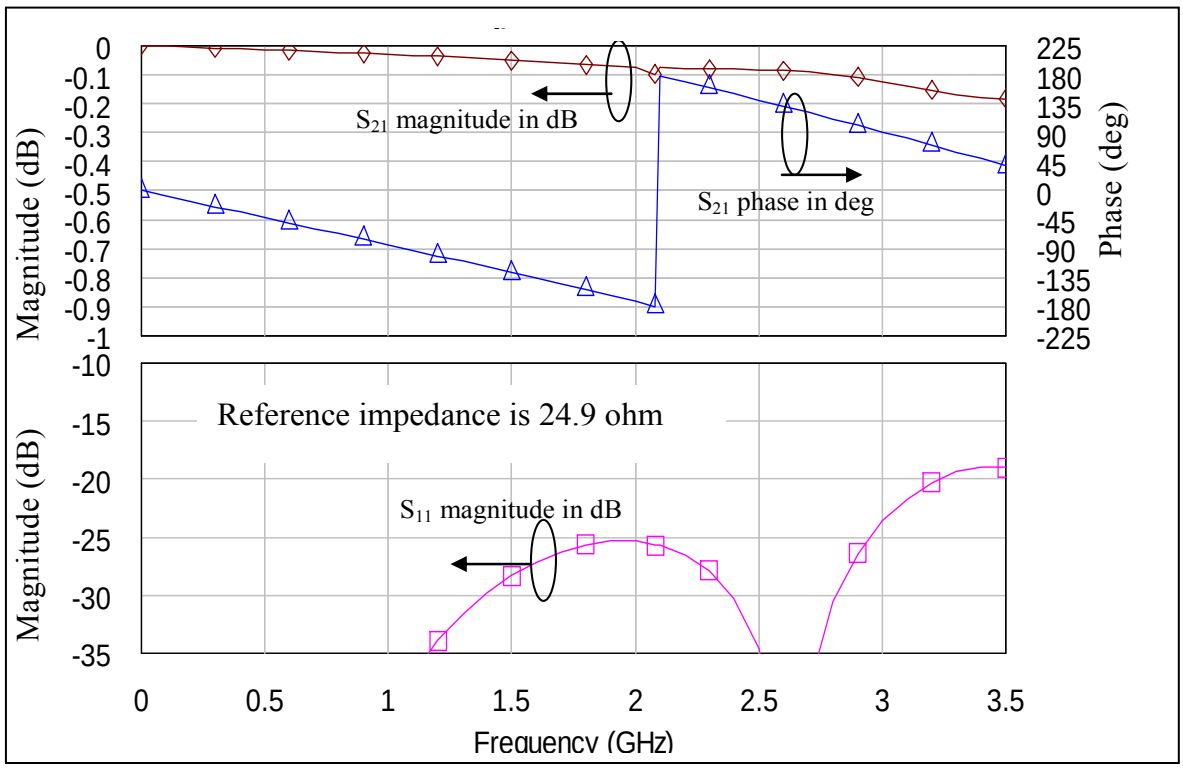



**Figure 4.17 EM simulated S-parameter responses of the 25 Ω ATL (Port reference impedance = 24.9 Ω).**

The magnitude of $S_{11}$ response in Fig. 4.17 suggests that the characteristic impedance of the ATL is 24.9 Ω. The phase of the ATL is 180° at 2.1 GHz. The structure shown in Fig. 4.16 was used for the final design.

## 4.6 ATL characterisation

For an ideal transmission line of characteristic impedance $Z_c$, the magnitudes of $S_{11}$ and $S_{22}$ will be zero (linear) and the magnitudes of $S_{21}$ and $S_{12}$ will be unity (linear) when tested in a system with reference impedance equal to the characteristic impedance. Using the same technique, the characteristic impedance of the DUT can be found out by adjusting the port reference impedance until best $S_{11}$ and $S_{22}$ responses are obtained and the characteristic impedance of the DUT will be the port impedance. However in the practical transmission line due to dispersion, the S-parameters will deviate from the ideal transmission line. In this project, to characterise the ATL an alternate approach was used.

Fig. 4.18 shows a transmission line with characteristic impedance $Z_c$, length $\ell$ and terminated with a reference impedance of $Z_o$. If the transmission line is tested in a reference system with the reference impedance $Z_o$ where $Z_o \neq Z_c$, then the S-parameter responses of the transmission line will be as shown in Fig. 4.19. It can be seen from Fig. 4.19 that the magnitude $S_{11}$ response contains uniform ripples with peaks and nulls. The peaks occur when $\ell$ is an odd multiple of quarter guide wavelength and nulls occur at integer multiples of half guide wavelengths.

With reference to Fig. 4.18, if $\ell = \lambda/4 + n\lambda/2$ for $n = 0, 1, 2, 3 \ldots$, the input impedance is given by [31]

$$Z_{in} = \frac{Z_c^2}{Z_o}. \tag{38}$$

$S_{11}$ can be written as,

$$S_{11} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o}. \tag{39}$$

Substituting, (38) in (39)

$$S_{11} = \frac{\frac{Z_c^2}{Z_o} - Z_o}{\frac{Z_c^2}{Z_o} + Z_o} = \frac{Z_c^2 - Z_o^2}{Z_c^2 + Z_o^2}. \tag{40}$$

The height of the ripple is equal to:

$$\left|S_{11}\right|_{L=\frac{m+1}{4}\lambda} = \left|\frac{Z_c{}^2 - Z_o{}^2}{Z_c{}^2 + Z_o{}^2}\right|; \; m = 0, 1, 2... \tag{41}$$

Conversely if the ripple height is known (eg. from the simulation or measurement), and if $Z_o$ is greater than $Z_c$, rearranging the equation (41) gives:

$$Z_c{}^2 = Z_o{}^2 \left[\frac{1 - |S_{11}|}{1 + |S_{11}|}\right]. \tag{42}$$

The magnitude of $S_{21}$ response is related to the magnitude of $S_{11}$ by the unity property for the lossless structures [31]:

$$|S_{21}| = \sqrt{1 - |S_{11}|^2}. \tag{43}$$

As an example, consider $Z_c = 25\ \Omega$, $\ell = 1.5\lambda$ at 2 GHz and $Z_o = 50\ \Omega$.

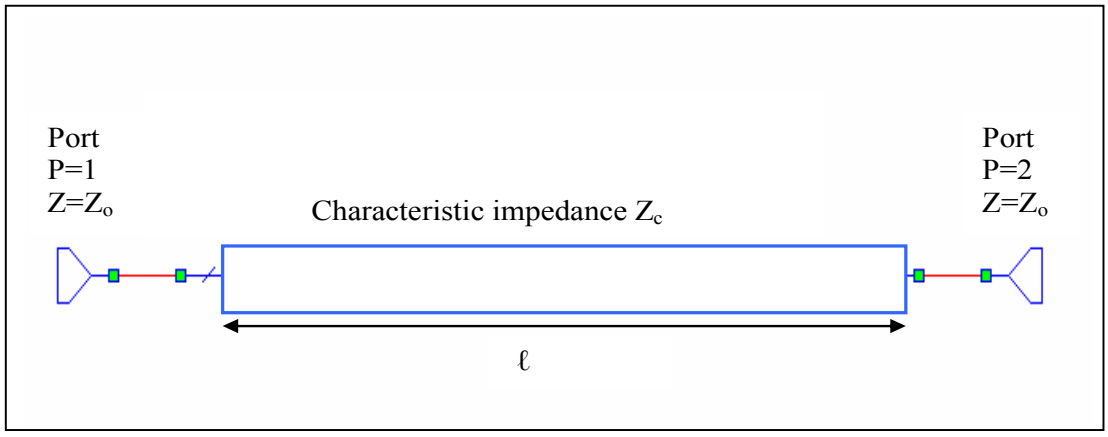



**Figure 4.18 Transmission line with characteristic impedance $Z_c$, length ℓ connected to ports with reference impedance $Z_o$.**

Fig. 4.19 shows the $S_{11}$ and $S_{21}$ responses of the transmission line with the characteristic impedance $Z_c$ equal to 25 Ω and the length equal to 1.5λ at 2 GHz. The reference impedance $Z_o$ is 50 Ω. The $S_{11}$ magnitude response shows the ripples of peak magnitude of -4.4 dB which is consistent with (41).

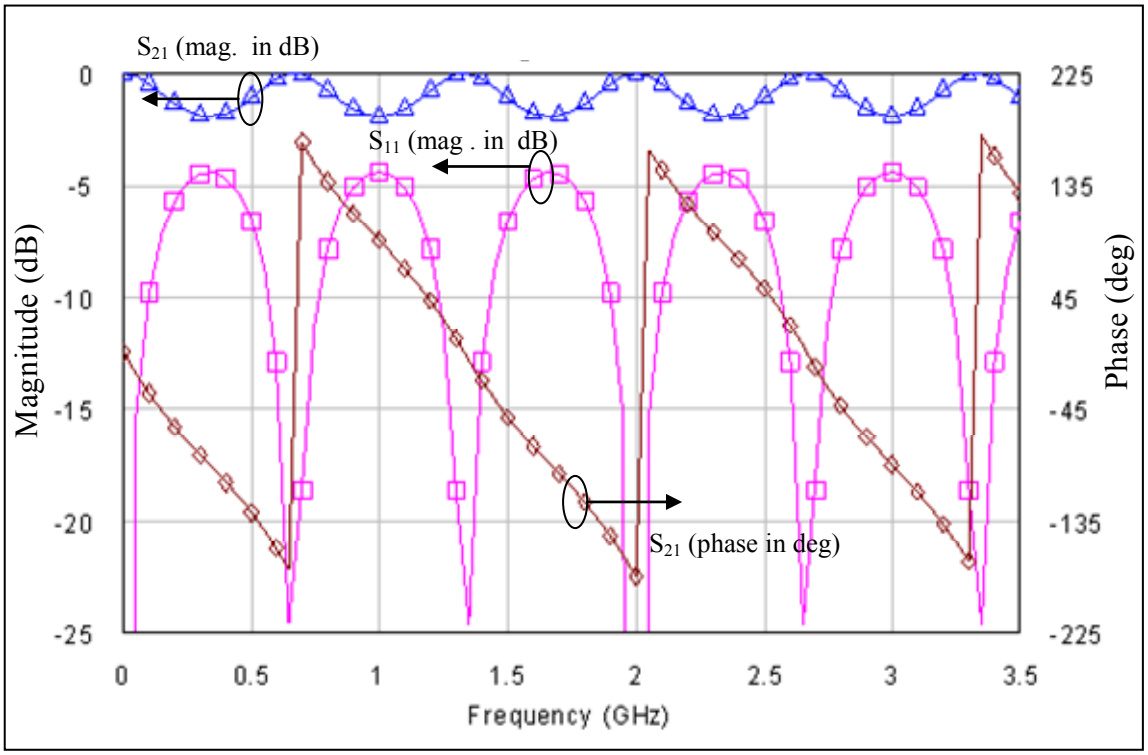



**Figure 4.19 Circuit simulated S-parameter responses of a transmission line with $Z_c$ = 25 Ω and length = 1.5λ at 2 GHz (Port reference impedance = 50 Ω).**

The same theory as detailed in section 4.6 was applied to find out the characteristic impedance of the 25 Ω ATL. Fig. 4.20 shows three 25 Ω ATLs with 180° electrical length (2.1 GHz) are cascaded. As explained earlier three ATL structures were required to get sufficient peaks in the band of interest. The reference impedance of the EM simulation setup was 50 Ω. The simulated S-parameter frequency response is shown in Fig. 4.21. It can be seen in Fig. 4.21 that the ripple height is -4.5 dB and using (42), the ATL characteristic impedance is 24.9 Ω. From the $S_{21}$ phase response, the electrical length of the ATL is 180° at about 2.1 GHz (in between 2 GHz and 2.1 GHz) and the

same is confirmed from the $S_{11}$ magnitude response (one of the nulls occurs at that frequency). The structure shown in Fig. 4.20 was used for the final layout.

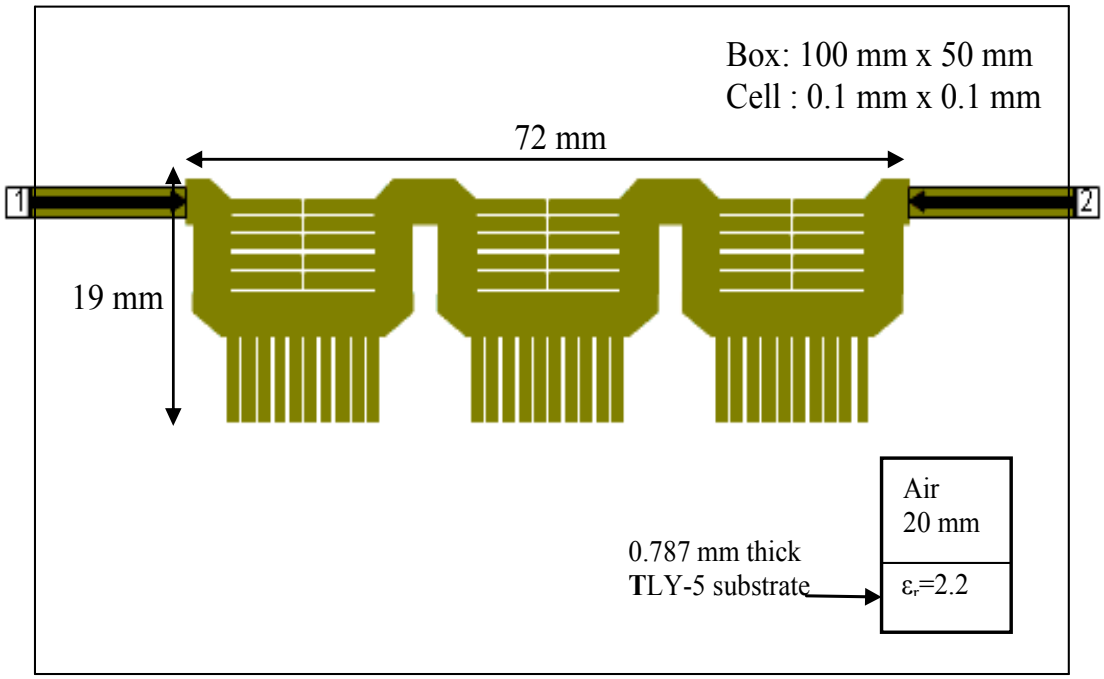



**Figure 4.20 EM simulation setup for three 25 Ω ATLs in cascade.**

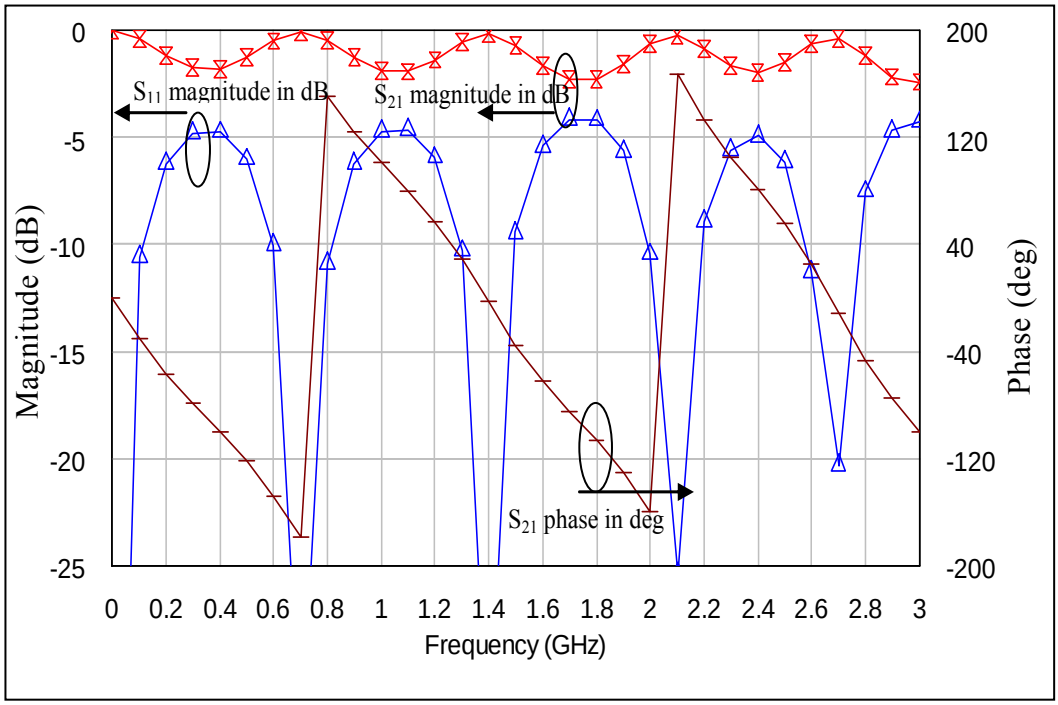



**Figure 4.21 EM simulated S-parameter responses of three 25 Ω ATLs in cascade (Port reference impedance = 24.9 Ω).**

## 4.7 Experiment description

### 4.7.1 Layout

The layout was generated using MWO and exported to CorelDRAW for adding text and mounting hole locators. The physical dimensions of the structure were not changed after the structure is exported to CorelDRAW. Two 15 mm long 50 Ω microstriplines were added at both ends of the ATL for soldering female SMA connectors. A separate 50 Ω microstripline was also added for modelling the female SMA connector and the SMA connector to microstrip discontinuity. The layout is shown in Fig. 4.22.

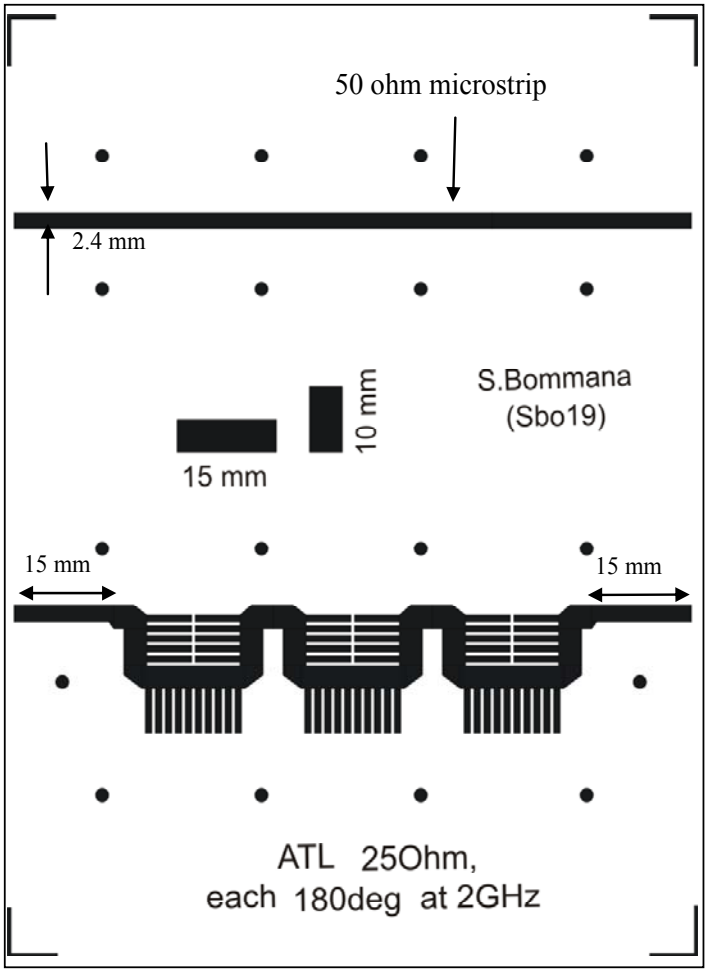



**Figure 4.22 Layout of three 25 Ω ATLs in cascade along with a 50 Ω microstripline.**

A double sided PCB was fabricated using Taconic TLY-5 substrate. The copper on the bottom of the PCB was not etched as it forms the ground plane. The PCB was fastened to an aluminium base plate using screws. The screws were sufficiently spaced from the ATL and the 50 Ω microstripline to avoid any coupling of the screws with the printed circuits. The SMA connectors were fastened to the base plate using the screws as shown in Fig. 4.23.

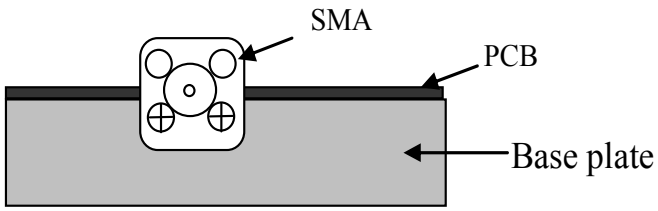



**Figure 4.23 SMA connector assembly on the base plate.**

The photograph in Fig. 4.24 shows the PCB and SMA connectors mounted on the base plate.

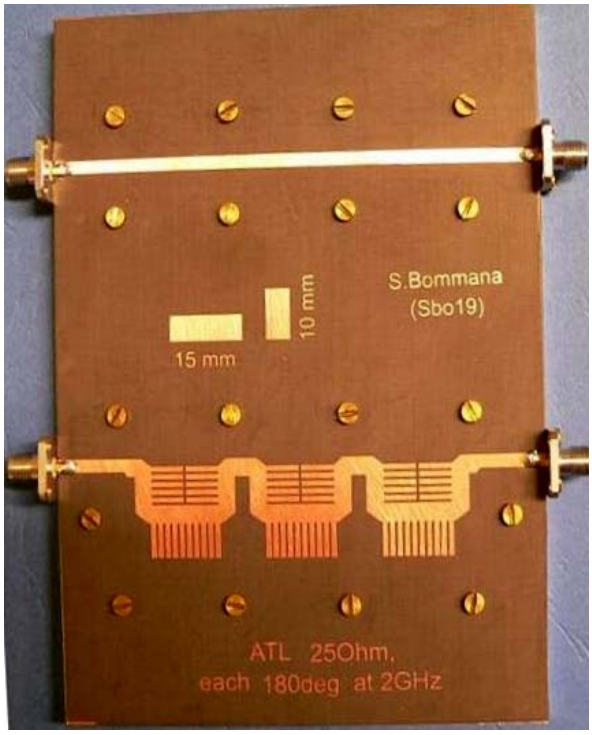



**Figure 4.24 Photo of the fabricated 25 Ω ATL along with the 50 Ω microstripline.**

### 4.7.2 Measurement setup

The S-parameter responses of the 25 Ω ATL were measured using the HP8753D Vector Network Analyser. The VNA was calibrated (full two port) using a 3.5 mm calibration kit prior to taking the measurements. The Short-Open-Load-Thru (SOLT) calibration method was used. The male SMA connectors of the VNA test port cables were torqued using a torque spanner. Fig. 4.25 shows the photo of the measurement setup for measuring the S-parameters of the 25 Ω ATL and the 50 Ω microstripline.

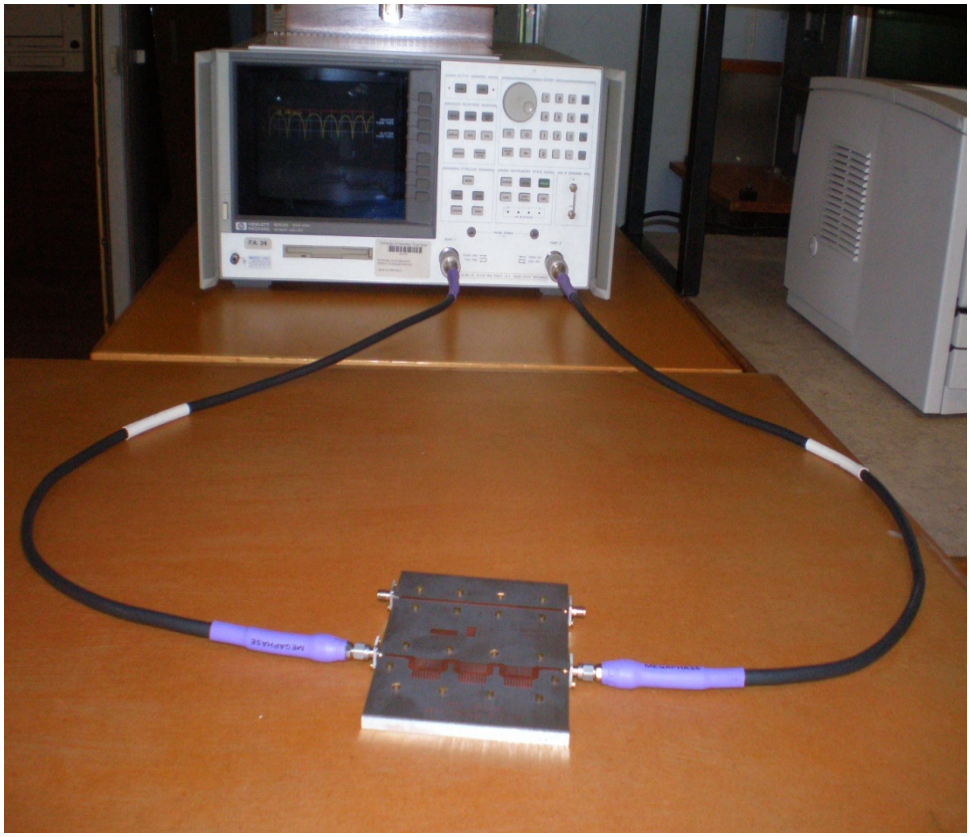


**Figure 4.25 Photo of the 25 Ω ATL measurement setup.**

### 4.7.3 Test fixture model

In this section modelling of the SMA connector and the discontinuity effects are described. The measurement setup for measuring the S-parameters of a DUT is shown

in Fig. 4.26. The measurement plane or the calibration plane is the point where the VNA has been calibrated. The measurement and the desired reference planes (DUT reference planes) are indicated in Fig. 4.26.

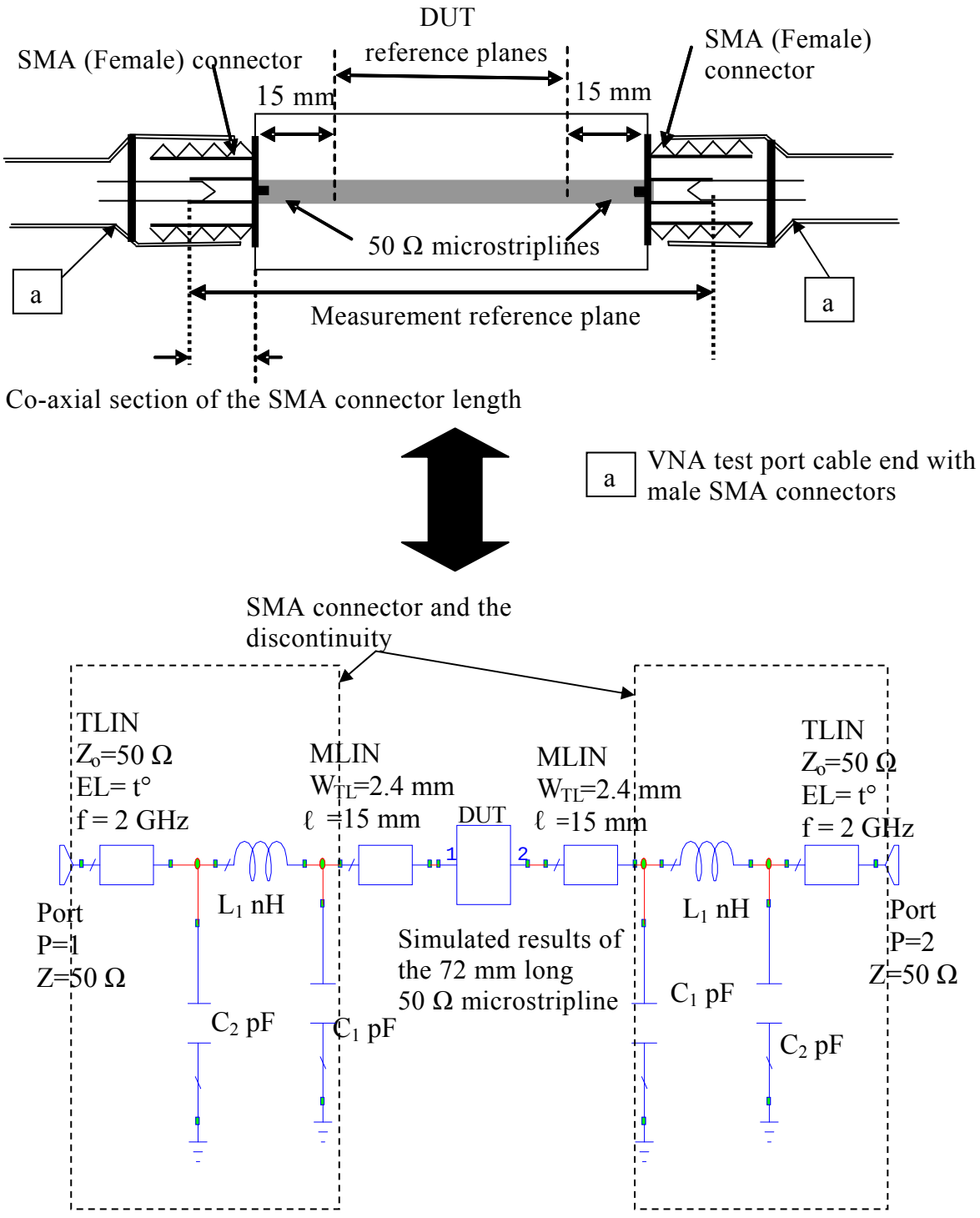



**Figure 4.26 Measurement setup and modelling of the 50 Ω microstrip through line.**

Fig. 4.26 also shows the schematic for modelling the SMA connector and the discontinuity arising due to the transition from the SMA connectors to the microstriplines. The port impedance of the modelled 2- port network is the reference impedance which is 50 Ω. The co-axial sections of the SMA connectors were modelled as 50 Ω transmission lines with an electrical length of $t°$ at 2 GHz. The co-axial section of the SMA connector is shown in Fig. 4.26. The LC pi sections in the schematic are for modelling the discontinuity. The 15 mm long microstriplines with the characteristic impedance of 50 Ω, added immediately before and after the DUT were for soldering the SMA connectors. The DUT contains the simulated data of the 50 Ω microstripline. The values of $L_1$, $C_1$, $C_2$ and $t$ were made as variables and optimised until the modelled S-parameter responses are same as the measured S-parameter responses. These optimised values will be used in de-embedding [35] the measured data.

### 4.7.4 De-embedding method

Fig. 4.27 shows the setup for de-embedding the measured data. The de-embedding process requires the values of $L_1$, $C_1$, $C_2$ and $t$ (Fig. 4.26) to be known. It can be seen in Fig. 4.27 that, in the process of de-embedding the measured data of the DUT, the SMA connector lengths ($t°$) were deducted from the measured data followed by the discontinuity and the 15 mm long 50 Ω microstriplines. The '-'sign before the values indicate the negating.

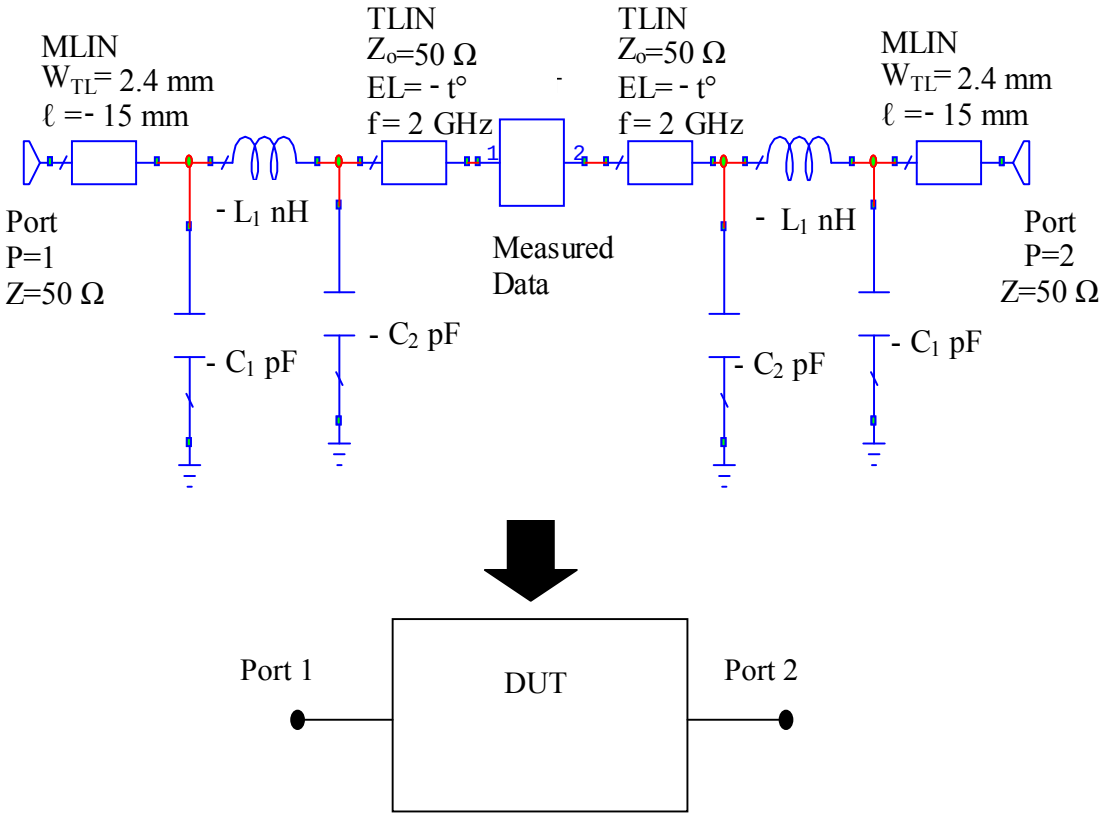
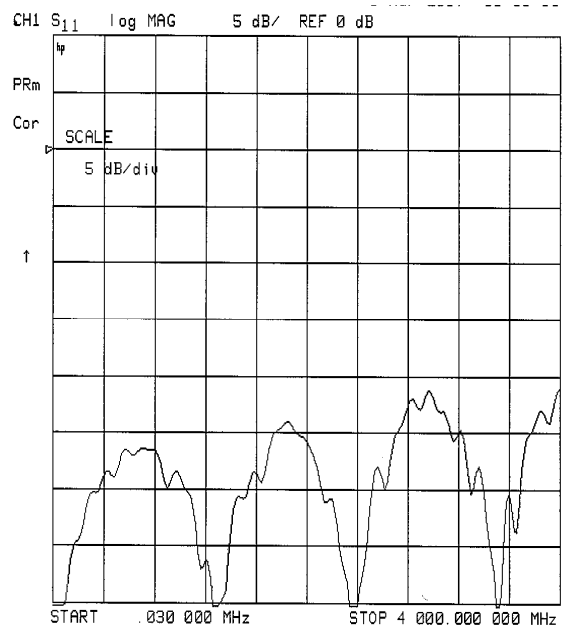



**Figure 4.27 Schematic for de-embedding the measured data of the DUT.**

## 4.8 Test fixture model optimisation

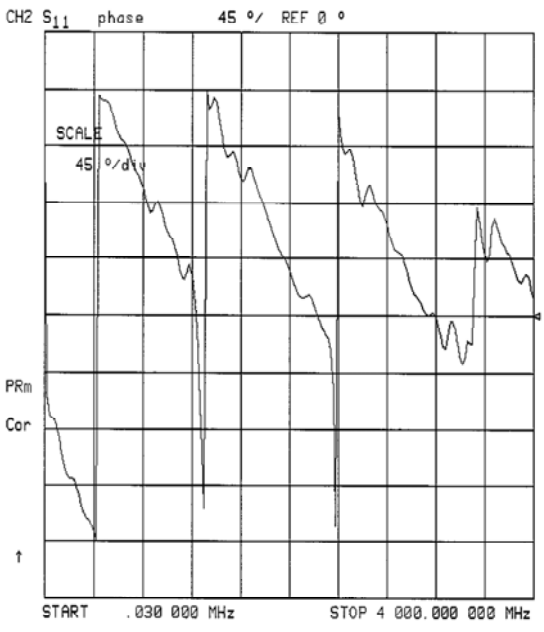
The raw measured S-parameter frequency responses of the 50 Ω microstripline are shown in Fig. 4.28. Only the $S_{11}$ (magnitude and phase) and $S_{21}$ (magnitude and phase) responses are shown in Fig. 4.28 as the DUT is symmetric.

Fig. 4.29 shows the measured S-parameter frequency responses and the optimised model simulation responses. The reference impedance is 50 Ω. The goals for the optimisation were set as the $S_{11}$ magnitude of the modelled data equal to the $S_{11}$ magnitude of the measured data and the $S_{21}$ phase of the modelled data equal to the $S_{21}$ phase of the measured data. The frequency range was 0 Hz to 3 GHz.



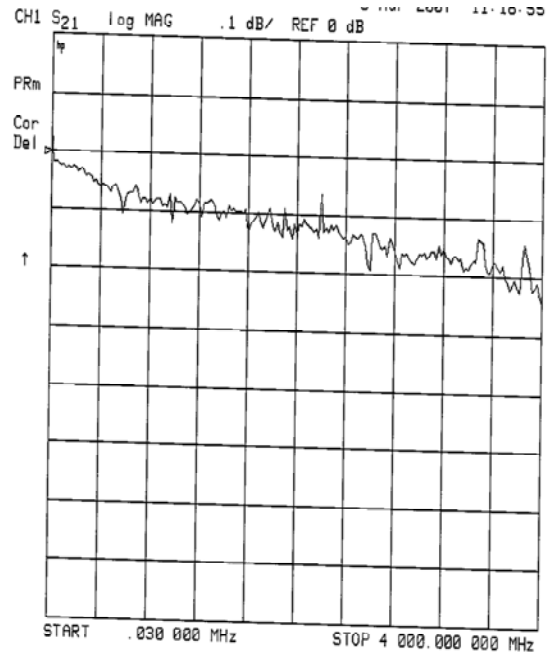

Magnitude of $S_{11}$ in dB

(a)



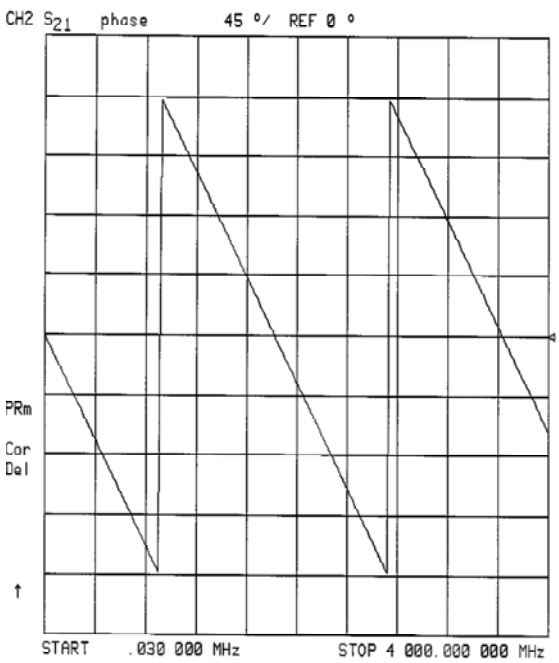

Phase of $S_{11}$ in degrees

(b)




Magnitude of $S_{21}$ in dB

(c)




Phase of $S_{21}$ in degrees

(d)

**Figure 4.28 Raw measured S-parameter responses of the 50 Ω microstripline. (a) $S_{11}$ magnitude (dB). (b) $S_{11}$ phase (deg). (c) $S_{21}$ magnitude (dB). (d) $S_{21}$ phase (deg).**

The optimised values of the pi network (discontinuity) are:

$L_1$ = 0.4583 nH,

$C_1$ = 0.1258 pF,

$C_2$ = 0.001404 pF.

The optimised value of the SMA connector (co-axial section) electrical length is:

$t$ = 27.4° at 2 GHz.

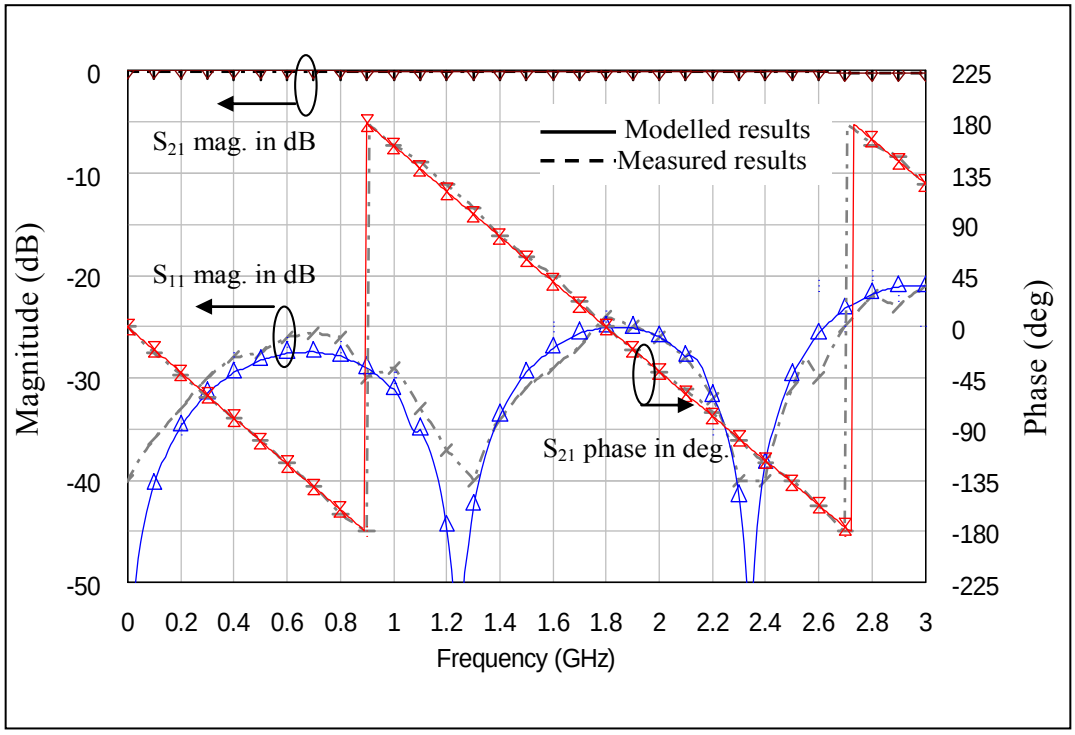
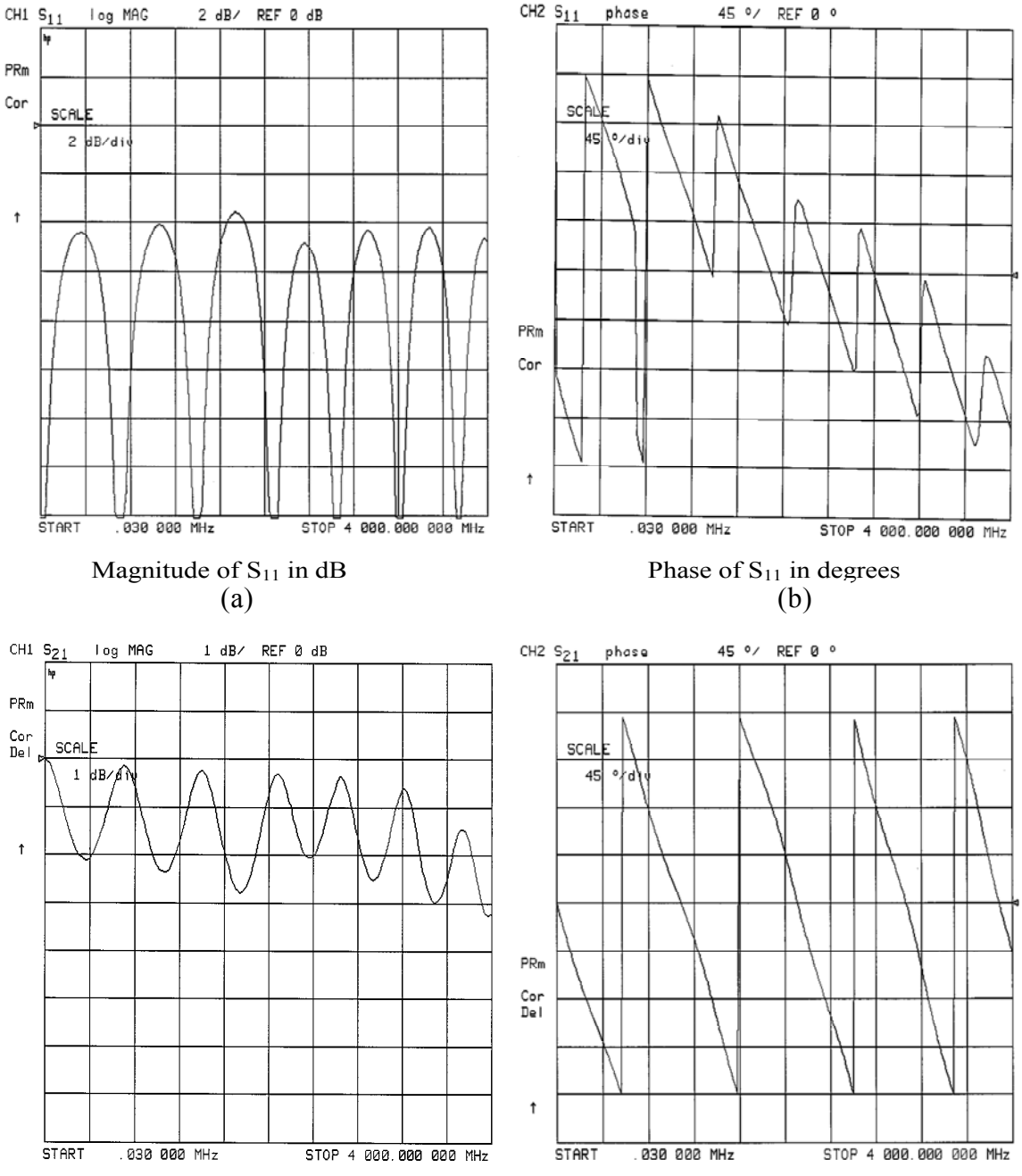



**Figure 4.29 Modelled and measured S-parameter responses of the 50 Ω test structure (Port reference impedance = 50 Ω).**

## 4.9 25 Ω ATL measurements

Fig. 4.30 shows the raw measured S-parameter responses of the 25 Ω ATL. Only the $S_{11}$ (magnitude and phase) and $S_{21}$ (magnitude and phase) responses are shown here as the ATL is symmetric.




Magnitude of $S_{11}$ in dB (a)

Phase of $S_{11}$ in degrees (b)

(c)

(d)

**Figure 4.30 Raw measured S-parameter responses of the 25 Ω ATL. (a) $S_{11}$ magnitude (dB). (b) $S_{11}$ phase (deg). (c) $S_{21}$ magnitude (dB). (d) $S_{21}$ phase (deg).**

For de-embedding the 25 Ω ATL measured data the schematic used is same as the schematic shown in Fig. 4.27. The measured raw data in Fig. 4.27 was the measured raw data of the 25 Ω ATL. The data assignment for the de-embedding is shown in table 4.2. The $S_{12}$ and $S_{22}$ measured data was made equal to $S_{21}$ and $S_{11}$ raw data because the 25 Ω ATL is symmetric.

| Data assignment for de-embedding | | |
|---|---|---|
| Measured data | | Raw data |
| $S_{11}$ | = | $S_{11}$ |
| $S_{21}$ | = | $S_{21}$ |
| $S_{12}$ | = | $S_{21}$ |
| $S_{22}$ | = | $S_{11}$ |

**Table 4.2 Data assignment for de-embedding the 25 Ω ATL measured data.**

The S-parameter frequency responses of the 25 Ω ATL de-embedded measurements are plotted along with the 25 Ω ATL EM simulated responses in Fig. 4.31. It can be seen in Fig. 4.31 that the 25 Ω ATL de-embedded measurement responses are similar to the EM simulated responses.

It can be seen in Fig. 4.31 that the $S_{11}$ magnitude response has peaks at -4.2 dB indicating that the characteristic impedance of the ATL is 24.4 Ω (using (42)). From the $S_{21}$ phase response in Fig. 4.31, the electrical length of the ATL is 180° at about 2.1 GHz (in between 2 GHz and 2.1 GHz). This is also confirmed from the $S_{11}$ magnitude response as one of the nulls occurs at the frequency. The S-parameter responses validate the design method used.

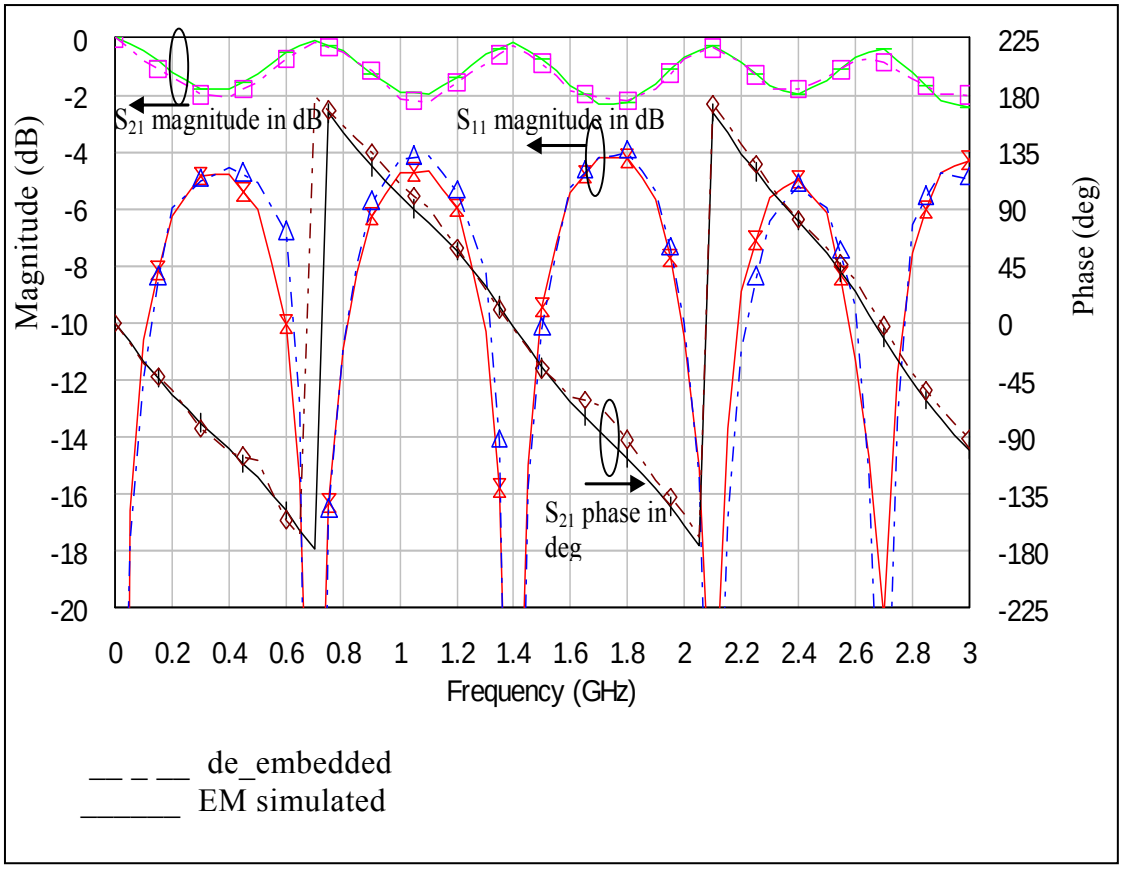



**Figure 4.31 De-embedded measured and EM simulated S-parameter responses of the 25 Ω ATL (Port reference impedance = 50 Ω).**

## 4.10 Size comparison

A normal 25 Ω microstripline with 180° electrical length on a PCB with substrate thickness of 0.787 mm, dielectric constant of 2.2, copper thickness of 0.017 mm and at 2 GHz will have a width of 6.15 mm and will be 53 mm long. Fig. 4.32 shows the 25 Ω meandered microstripline.

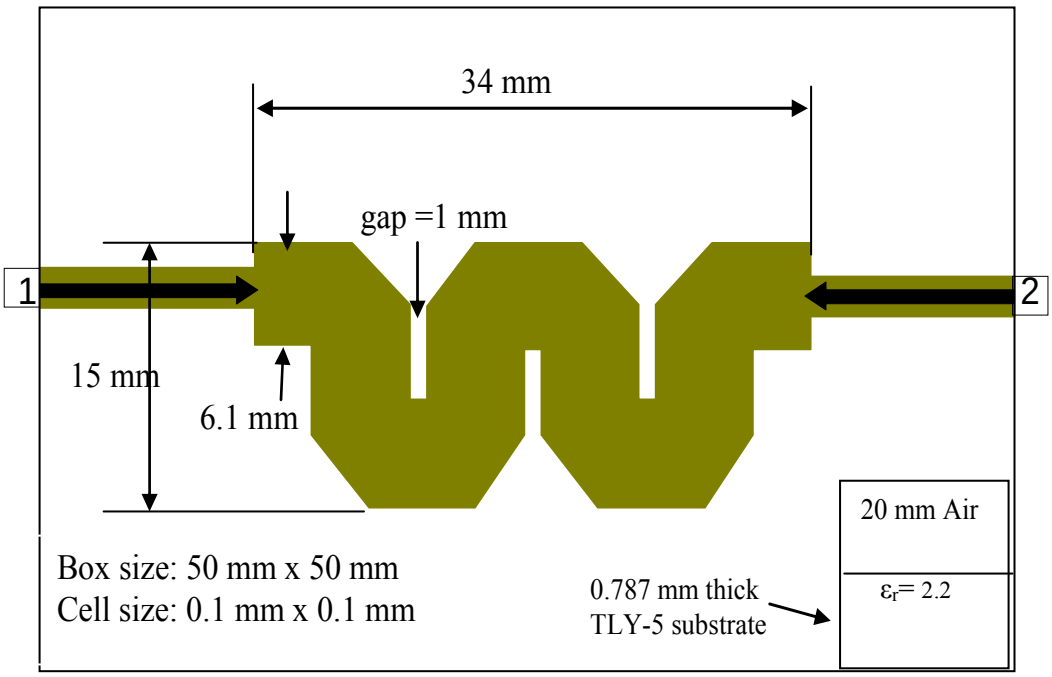



**Figure 4.32 A 25 Ω meandered microstripline.**

The meandered microstripline with a gap of 2.4 mm (3 times substrate thickness) was EM simulated. For further size reduction the meandered microstripline with 1 mm gap was also EM simulated. The meandered microstripline shown in Fig. 4.32 is with 1 mm gap. The box and cell size for the EM simulation are shown in Fig. 4.32. The S-parameter responses of the meandered microstriplines with gaps 2.4 mm and 1 mm are shown in Fig. 4.33.

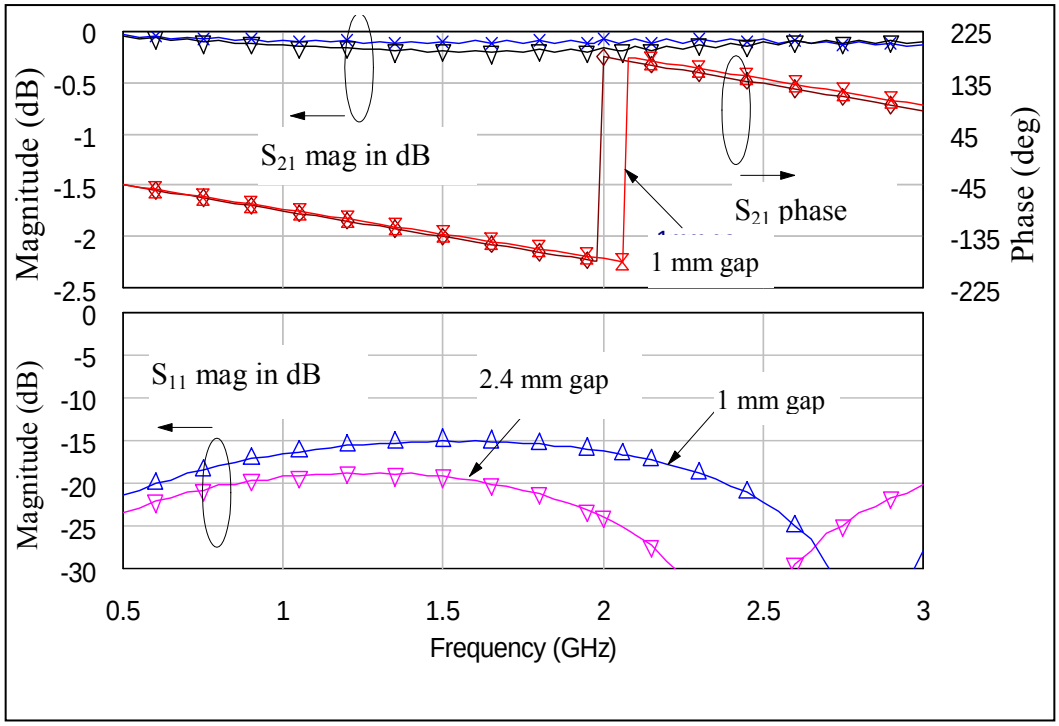



**Figure 4.33 EM simulated S-parameter responses of the 25 Ω meandered microstriplines.**

Comparing the meandered microstriplines S-parameter frequency responses in Fig. 4.33 with the EM simulated S-parameter frequency responses of the 25 Ω ATL (Fig. 4.17), it can be concluded that the ATL has a better response compared to the meandered microstriplines. This confirms that the meander lines suffer from the coupling between adjacent bends and the bends limit the bandwidth. Though the scales of the two figures (Fig. 4.17, Fig. 4.33) are different the magnitudes of $S_{11}$ can be compared.

Size of the 25 Ω ATL with 180° electrical length (2.1 GHz) = 22 mm x 19 mm = 418 sq. mm. Size of the 25 Ω meandered microstripline with 180° electrical length (2 GHz) = 34 mm x 15 mm = 510 sq. mm. The design of the 25 Ω ATL resulted in 18% reduction in area compared to the meandered microstripline.

# CHAPTER FIVE

## 7 Ω ARTIFICIAL TRANSMISSION LINE

### 5.1 Introduction

A 7 Ω microstripline will have a width of 27 mm on a 0.787 mm thick substrate with a dielectric constant of 2.2 and at 2 GHz. The width is close to $\lambda_g/4$ at 2 GHz and such a wide microstripline will have problems with higher order modes [36] and would not behave as a one-dimensional transmission line at 2 GHz. The design of a 7 Ω transmission line with electrical length of 90° at 2 GHz using the ATL concept to reduce the size of the transmission line is discussed in this chapter. A 0.787 mm thick TLY-5 substrate with a dielectric constant of 2.2 was used for the ATL fabrication.

It will be shown that ATLs with characteristic impedance less than 10 Ω are difficult to realise. It will also be shown that, to realise such a low characteristic impedance ATL, two identical ATLs are connected in parallel with characteristic impedance twice that of the desired characteristic impedance i.e. to realise a 7 Ω ATL, two 14 Ω ATLs will be connected in parallel. The parametric analysis was carried out to find out the most suitable parameters for realising the 7 Ω ATL and the details of the analysis is given in section 5.2. The circuit simulation for the 7 Ω ATL is described in section 5.3 and the experimental description and the results are given in section 5.4.

### 5.2 Parametric analysis

In this analysis the relation between the parameters of the ATL is studied to find a suitable width of the microstrip, the shunt capacitance required and the length of the

unit cell for realising a 7 Ω ATL. The parameters used for the analysis were, $\Phi_{ATL} = 90°$ at 2 GHz, $h$ = 0.787 mm, $Z_{oATL}$ = 7 Ω and $\varepsilon_r$ = 2.2. The analysis was carried out with imposed constraints such as the minimum width of the microstripline 0.5 mm (fabrication limitation) and the maximum stub length of $0.1\lambda_g$.

### 5.2.1 Relation between d and $W_{TL}$

Using (24) the relation between $d$ and $W_{TL}$ for various values of $N$ is shown in Fig. 5.1. Fig. 5.2 shows the various labels used in equation (24). If a stub with 0.5 mm width is chosen and if the spacing between the stubs is 0.6 mm, then a minimum $d$ of 1.1 mm is required. The dark thick line in Fig. 5.1 is for $d$ =1.1 mm. It can be observed in Fig. 5.1 that, $N$ =19 to 25 cannot be used as $d$ will become less than 1.1 mm.

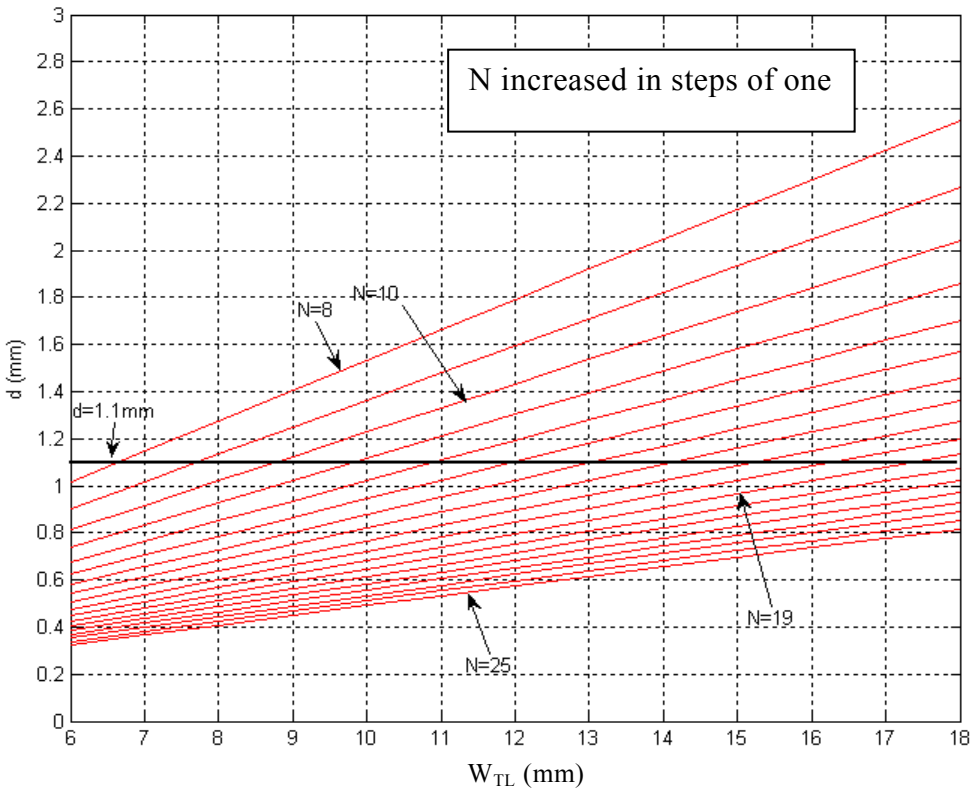



**Figure 5.1 Plot of d versus $W_{TL}$ for a 7 Ω ATL.**

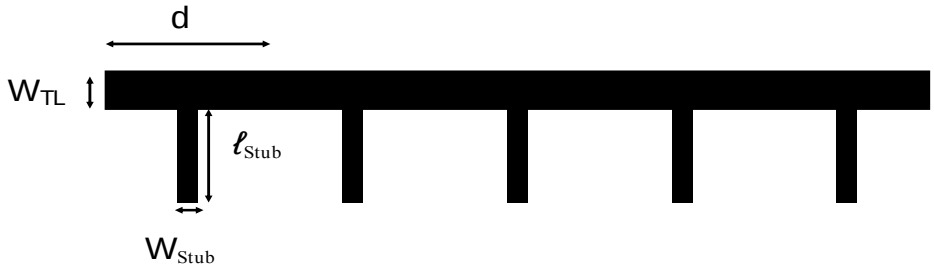



**Figure 5.2 A typical ATL structure.**

### 5.2.2 Relation between $C_p$ and $W_{TL}$

If the stubs are placed on both sides of the microstripline as shown in Fig. 5.3, then the required stub capacitance will be halved and that means short stubs can be used. Equation (27) can be written as:

$$C_p = \frac{\Phi_{ATL}(Z_{oTL}^2 - Z_{oATL}^2)}{2N\omega Z_{oTL}^2 Z_{oATL}} \tag{44}$$

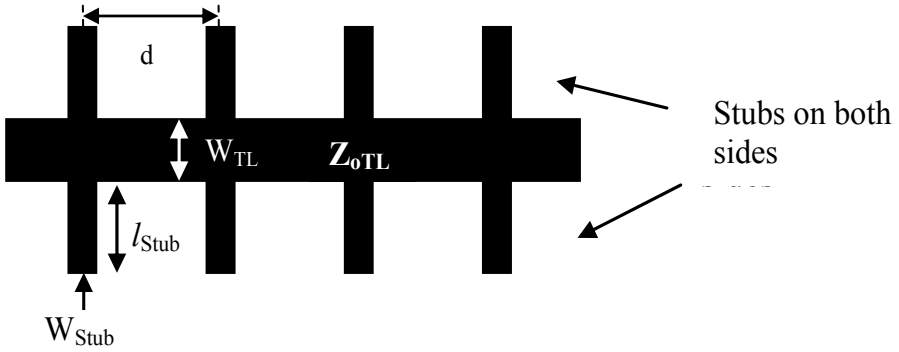



**Figure 5.3 ATL with stubs on both sides.**

Using (44) the relation between $C_p$ and $W_{TL}$ for various values of $N$ is shown in Fig. 5.4. It can be seen in Fig. 5.4 that for an ATL with the same characteristics, if $W_{TL}$ is increased then a small value of the shunt capacitance can be used. From Fig. 5.4, the capacitance that can be used is 0.3 pF with $W_{TL}$ equal to 18 mm and $N$ equal to 17,

which is very small. That means to achieve a small capacitance $W_{TL}$ and $N$ have to be large. With large $W_{TL}$ there can be problems associated with higher mode excitations.

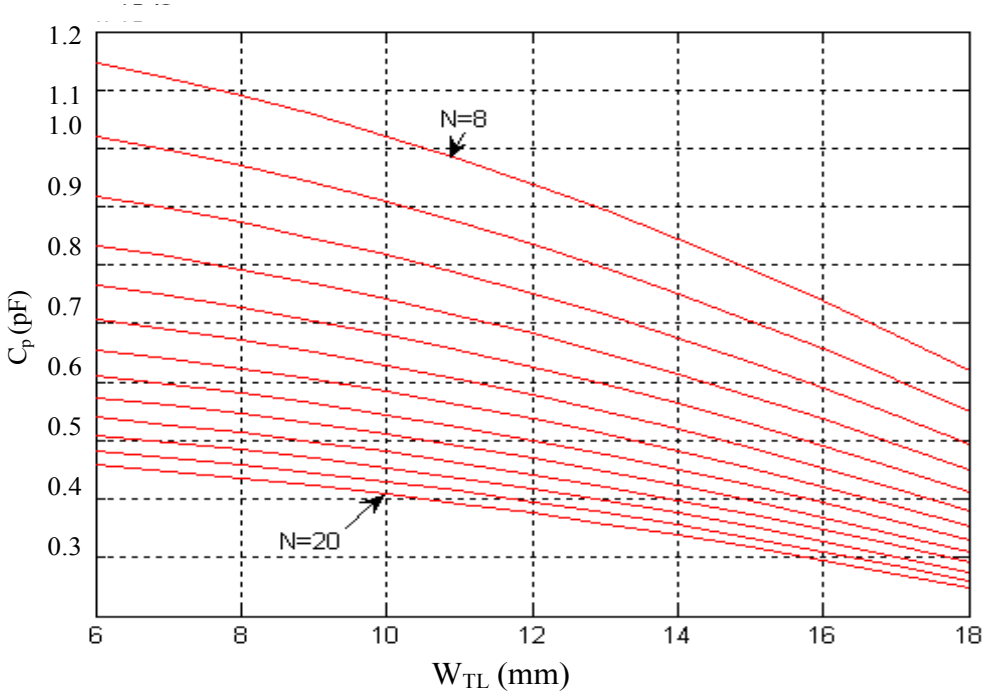



**Figure 5.4 Plot of $C_p$ versus $W_{TL}$ for a 7 Ω ATL.**

### 5.2.3 Relation between $\ell_{Stub}$ and $W_{Stub}$

Using (30) the relationship between $W_{Stub}$ and $\ell_{Stub}$ for various values of $W_{TL}$ and $N$ equal to 18 is shown in Fig. 5.5. The maximum stub length is limited to $0.1\lambda_g$ which is shown with a dark line. It can be seen in Fig. 5.5 that, if the stub length is limited to $0.1\lambda_g$ and if the range of $W_{TL}$ is between 6 mm to 12 mm (small $W_{TL}$ is better), then the stub width will be more than 1.5 mm. But the width of the stub has to be smaller than the $d$. Also, increase of the stub width means an increase in $d$ and that results in, an increase in the ATL length. It can be seen in Fig. 5.1 that if d is increased to more than 1.5 mm, then $N$ has to be limited to 14 and below. If $N$ is reduced to 14, then a large $W_{TL}$ is required to limit the stub length below $0.1\lambda_g$.

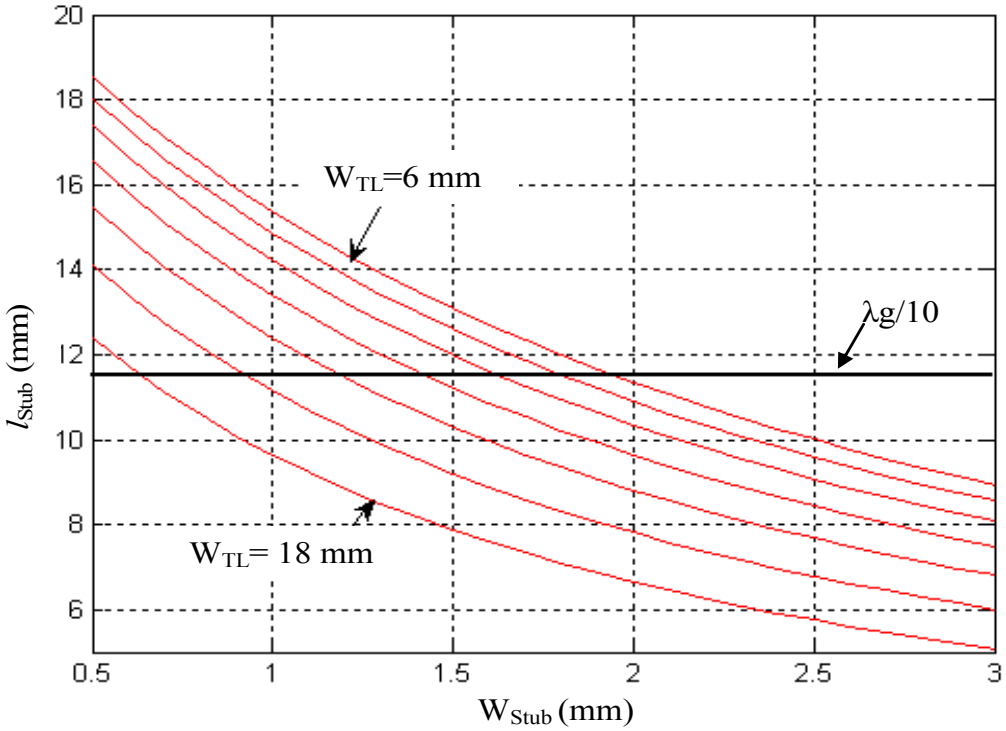



**Figure 5.5 Plot of $\ell_{Stub}$ versus $W_{Stub}$ for a 7 Ω ATL.**

The parametric analysis done so far is summarised as:

From Fig. 5.1, $N$ cannot be more than 18 as $d$ will be less than 1.1 mm (stub width 0.5 mm). From Fig. 5.4, for $N$ =18, the capacitance required will be large if small $W_{TL}$ is used and large capacitance means long and wide stubs which results in increase in the ATL size. Also from Fig. 5.4, with $W_{TL}$ equal to 18 mm, the required stub capacitance is 0.3 pF which is very small, but large widths ($W_{TL}$) are at risk from higher mode excitations. From Fig. 5.5, if a small $W_{TL}$ is used to realise the ATL, then long stubs are required which violates the maximum length constraint ($0.1\lambda_g$). From the parametric analysis done so far, it can be concluded that there is a conflict in choosing the parameter values to realise a compact 7 Ω ATL structure. To realise a compact ATL structure, use of lumped capacitors in place of stubs is considered. The parametric analysis was extended to find out the parameter values of $W_{TL}$ and $C_p$ (lumped) for realising the 7 Ω ATL.

### 5.2.4 Relation between $Z_{oATL}$ and $W_{TL}$ with varying $C_p$

Substituting the values of $L$ and $C$ from (3) and (4) in (18)

$$Z_{oATL} = \sqrt{\frac{Z_{oTL}}{v_{pTL}\left(\frac{1}{Z_{oTL}v_{pTL}} + \frac{C_p}{d}\right)}} \,. \tag{45}$$

Using (45) the relation between $Z_{oATL}$ and $W_{TL,}$ for various values of $C_p$ is shown in Fig. 5.6. The lumped capacitors used in this project were of 0603 size, i.e. 1.6 mm long and 0.8 mm wide. If two capacitors are placed with 1 mm spacing between them as shown in Fig. 5.7, then a minimum $d$ of 1.8 mm is required. So the $d$ was fixed at 2 mm for this parametric analysis.

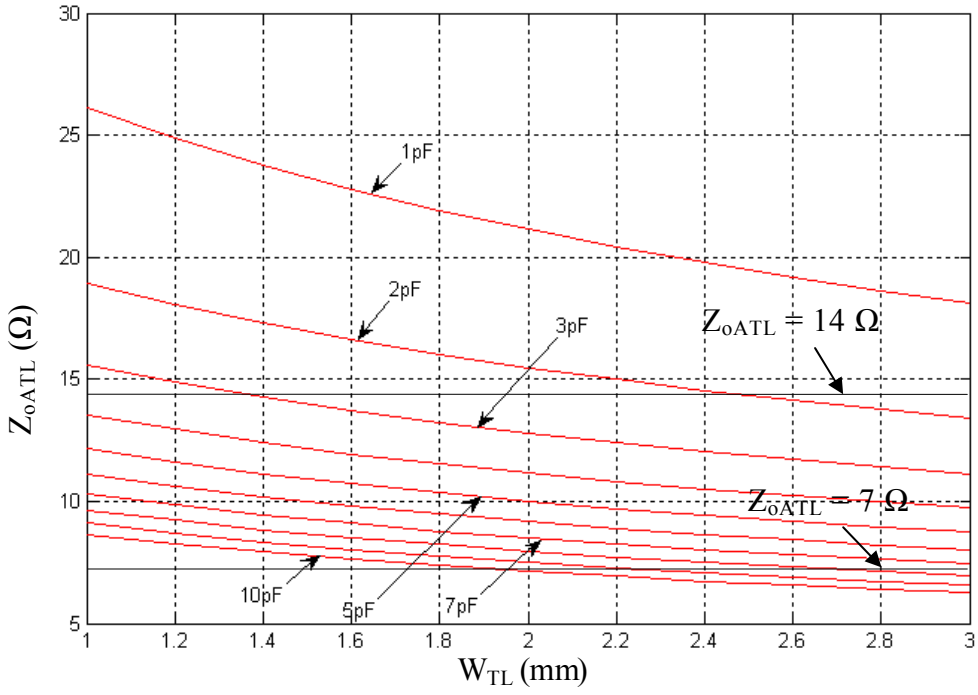



**Figure 5.6 Plot of $Z_{oATL}$ versus $W_{TL}$ for different values of $C_p$ for d = 2 mm.**

It can be seen in Fig. 5.6 that a small characteristic impedance ATL can be realised with a large value of shunt capacitance. The two dark lines in Fig. 5.6 indicate $Z_{oATL}$

equal to 14 Ω and 7 Ω. It can be seen in Fig. 5.6 that, for $Z_{oATL}$ equal to or less than 10 Ω, the change in $W_{TL}$ has a very small affect for the same value of capacitance.

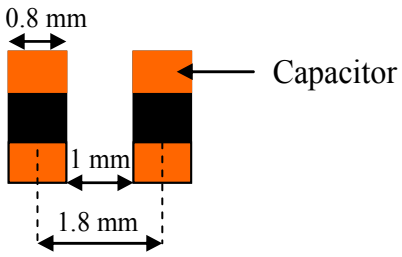



**Figure 5.7 Two 0603 size capacitors with 1 mm spacing.**

### 5.2.5 Relation between $Z_{oATL}$ and $W_{TL}$ with varying N

Equation (24) can be written as:

$$Z_{oATL} = \frac{\omega Z_{oTL} N d}{\Phi_{ATL} v_{pTL}}. \qquad (46)$$

Using (46) the relation between $Z_{oATL}$ and $W_{TL}$ for various values of $N$ is shown in Fig. 5.8. The two dark lines indicate $Z_{oATL}$ equal to 14 Ω and 7 Ω.

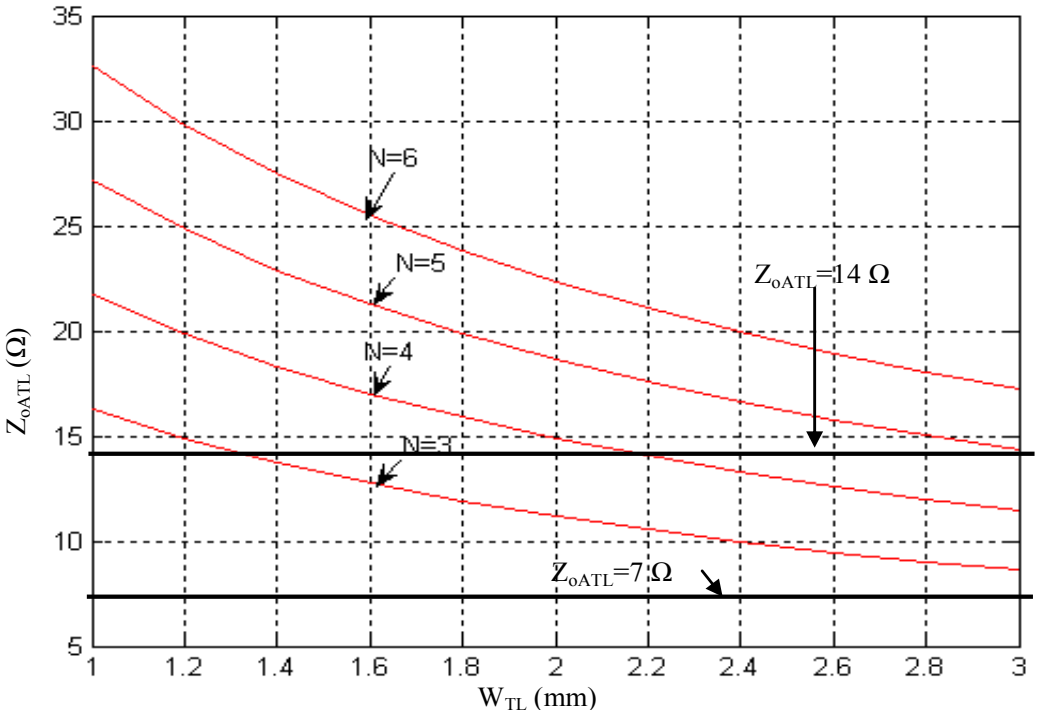



**Figure 5.8 Plot of $Z_{oATL}$ versus $W_{TL}$ for different values of N.**

From Fig. 5.8 it can be seen that, $N$ should be less than 3 to realise a 7 Ω ATL. From Fig. 5.6 and Fig. 5.8 it is evident that realising a 7 Ω ATL is difficult using the current methods. So to realise a 7 Ω ATL an alternate approach was chosen. A 7 Ω ATL can be realised by connecting two 14 Ω ATLs in parallel. To realise a 14 Ω ATL the values of $W_{TL}$, shunt capacitance value ($C_p$) and number of shunt capacitors ($N$) can be read from Fig. 5.6 and 5.8. The capacitor values available for this project are 1 pF, 2 pF, 4.7 pF and 10 pF. With the available values of capacitors, $d$ and $N$ are calculated using (24) and (27), and tabulated in table 5.1. $W_{TL}$ was 2.4 mm.

| $C_p$ | $N$ | $d$ |
|---|---|---|
| 1 pF | 9 | 1 mm |
| 2 pF | 4 | 2.1 mm |
| 4.7 pF | 2 | 4.7 mm |
| 10 pF | 1 | 10 mm |

**Table 5.1 N and d values for various $C_p$ values for realising a 14 Ω ATL.**

The values of $C_p$ equal to 1 pF cannot be used as $d$ cannot be less than 1.8 mm (Fig. 5.7) and $C_p$ equal to 4.7 pF and 10 pF cannot be used as $N$ has to be less than 3. So $C_p$ = 2 pF was chosen and the final parameter values used for realising the 14 Ω ATL are shown in table 5.2.

| Parameter | Value |
|---|---|
| $W_{TL}$ | 2.4 mm |
| $N$ | 4 |
| $C_p$ | 2.0 pF |
| $d$ | 2.1 mm |

**Table 5.2 Parameter values for realising a 14 Ω ATL.**

## 5.3 Circuit simulation

The parameters values obtained (Table 5.2) were used for the circuit simulation. Fig. 5.9 shows the schematic of the 14 Ω ATL.

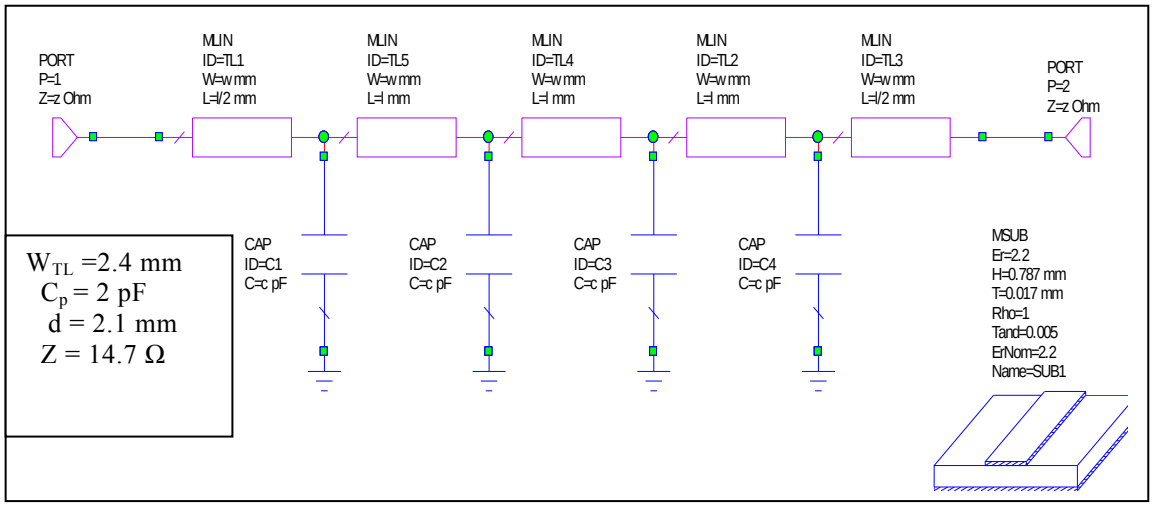



**Figure 5.9 Schematic of the 14 Ω ATL.**

Fig. 5.10 shows the S-parameter simulation response of the circuit shown in Fig. 5.9. The $S_{11}$ magnitude response shows that the characteristic impedance of the ATL is close to the reference impedance, 14.7 Ω and the phase is close to 90° at 2 GHz.

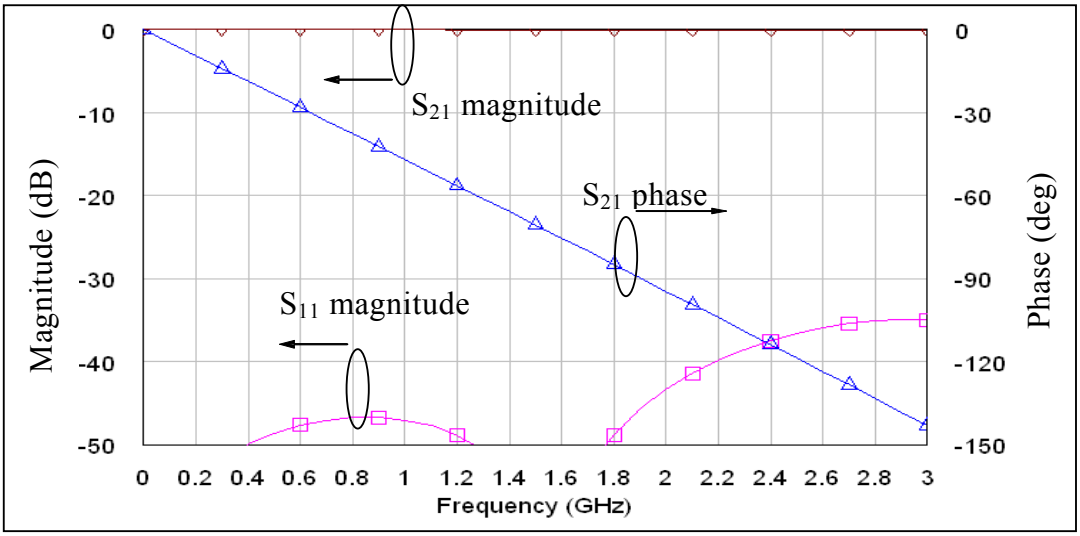



**Figure 5.10 Circuit simulated S-parameter responses of the 14 Ω ATL (Port reference impedance = 14.7 Ω).**

To obtain a characteristic impedance of 7 Ω, two 14 Ω ATLs were connected in parallel. The schematic in Fig. 5.11 shows two 14 Ω ATLs connected in parallel. The S-parameter frequency response is shown in Fig. 5.12.

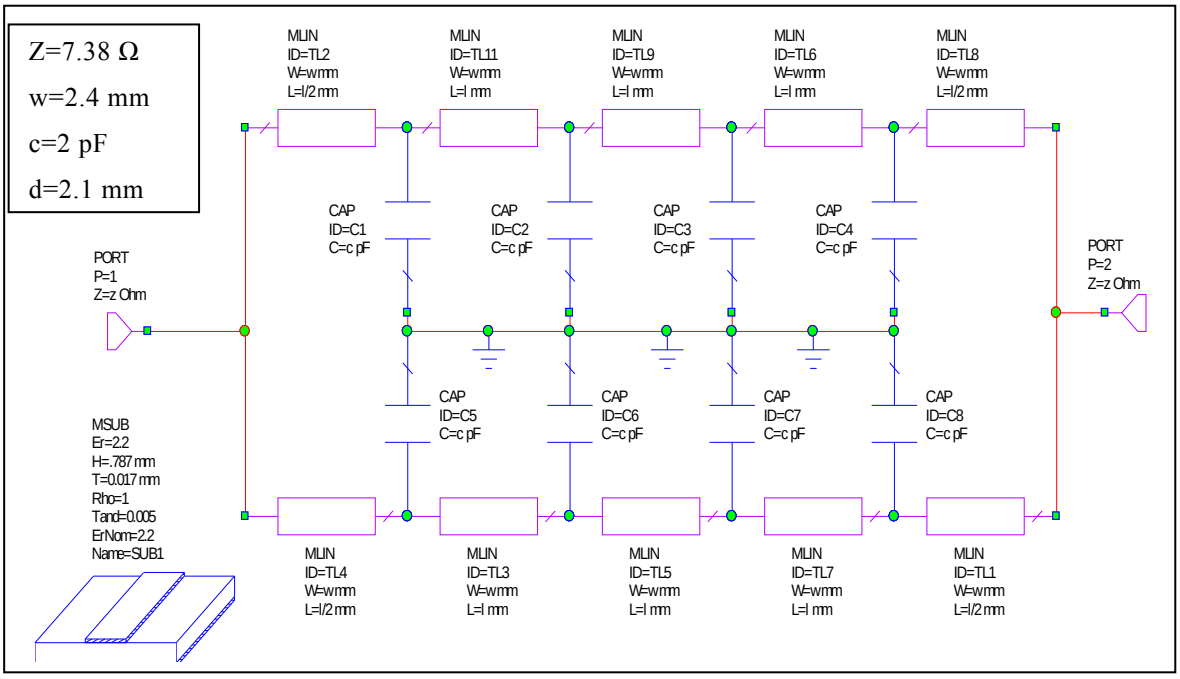



**Figure 5.11 Schematic of two 14 Ω ATLs in parallel.**

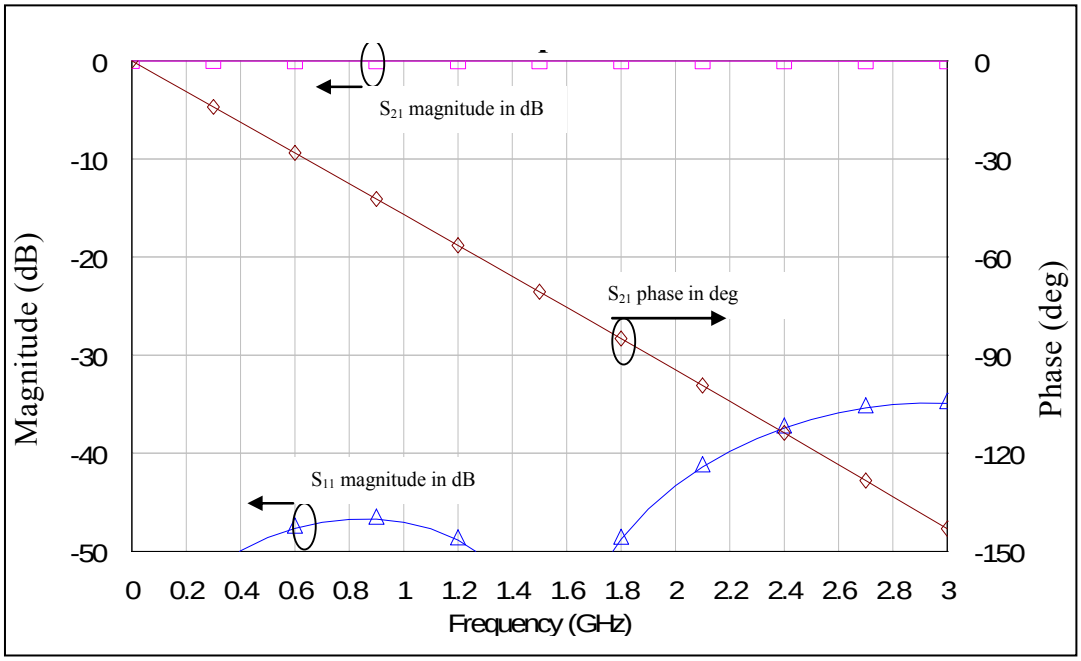



**Figure 5.12 Circuit simulated S-parameter responses of two 14 Ω ATLs in parallel (Port reference impedance = 7.38 Ω).**

The $S_{11}$ magnitude response in Fig. 5.12 shows that the 7 Ω ATL can be realised by connecting two 14 Ω ATLs in parallel.

Generally capacitors have parasitic inductances. The 2 pF capacitors used in this project are from American Technical Ceramic (ATC), and are 600S series chip capacitors. From the data sheet attached in Appendix 2, the self resonance frequency of a 2 pF capacitor is about 8.4 GHz and that means the parasitic inductance of the capacitor is 0.178 nH.

The circuit simulation was carried out with the capacitors with their parasitic inductances. The schematic is shown in Fig. 5.13.

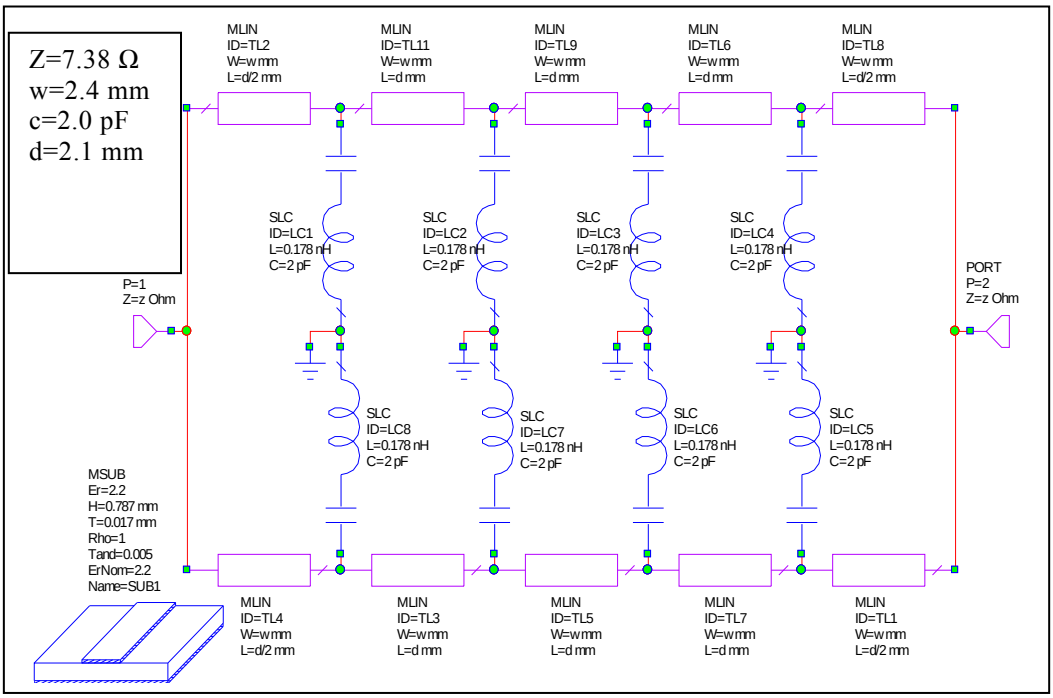



**Figure 5.13 Schematic of the 7 Ω ATL with 2 pF capacitors and its parasitic inductance.**

The circuit simulation S-parameter frequency response is shown in Fig. 5.14. The $S_{11}$

magnitude response in Fig. 5.14 indicates that the characteristic impedance of the ATL is close to the port reference impedance 7.38 Ω.

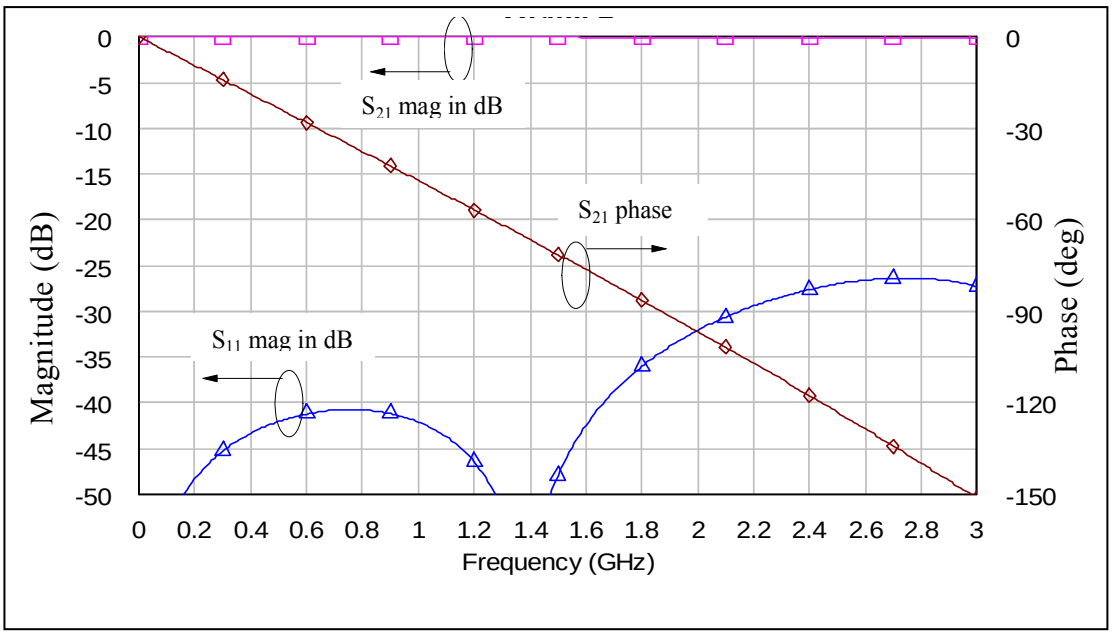



**Figure 5.14 Circuit simulated S-parameter responses of the 7 Ω ATL with capacitors with parasitic inductances (Port reference impedance 7.38 Ω).**

### 5.3.1 Layout Geometry

The layout geometry for the 7 Ω ATL is shown in Fig. 5.15. The length of the ATL is 8.4 mm and the width is 7 mm. The capacitors were placed inwards to achieve a compact structure. The two 2.4 mm main microstriplines were connected together with a 0.2 mm microstrip as shown in Fig. 5.15.

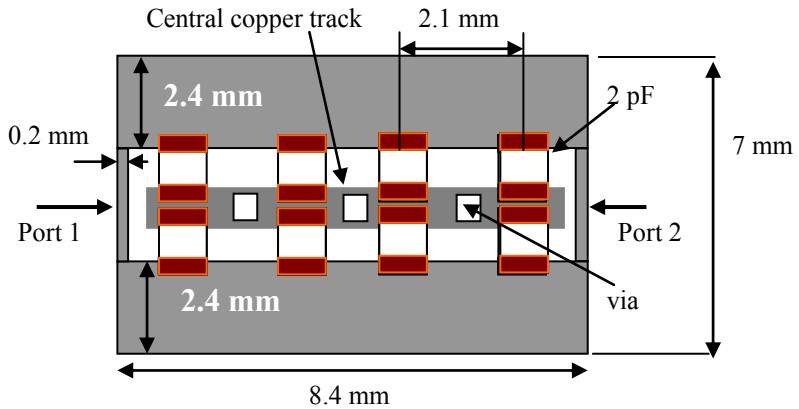



**Figure 5.15 7 Ω ATL layout geometry.**

One end of the capacitor was soldered to the main microstrip (2.4 mm) and the other end was soldered to the 1 mm wide microstrip in the centre as shown in Fig. 5.16. In Fig. 5.15, the vias on the central microstrip (in the middle) were required to connect the central microstrip to the bottom ground layer to give the ground connection for the capacitors. Three vias were used for the grounding requirement as shown in Fig 5.15.

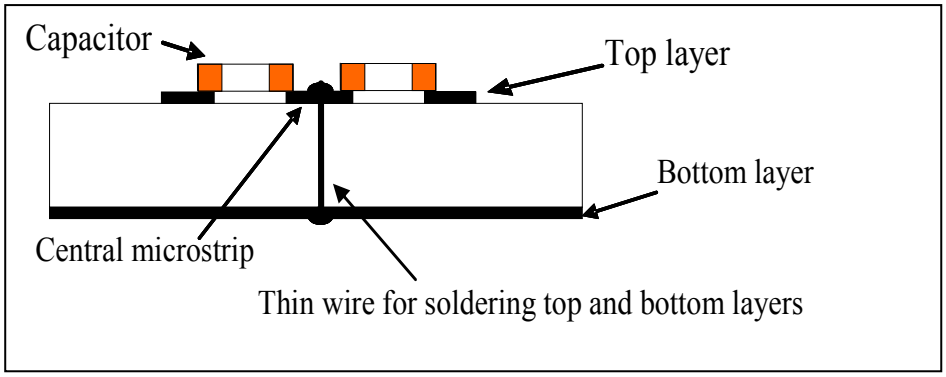



**Figure 5.16 Assembly of the capacitors.**

The width of the central microstrip cannot be reduced any further, because two capacitors have to be soldered on the microstrip as shown in Fig. 5.16. A gap of 0.6 mm was maintained all around the central microstrip (ground) to avoid any coupling.

A double sided PCB was fabricated and the bottom layer was not etched and kept for the ground plane. The PCB was fastened to an aluminium base plate using screws, and the SMA connectors were screwed onto the base plate as shown in Fig. 5.17.

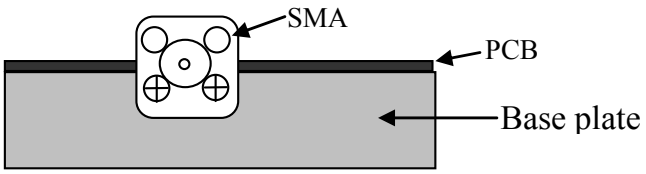



**Figure 5.17 Assembly of the SMA connector on base plate.**

The resources to fabricate printed through holes (via) were not available so thin wires were inserted through the three via holes (ref Fig. 5.16) and soldered at top and bottom layers of the PCB for grounding requirements. It is important that the PCB and the base plate make good contact so that common ground is maintained. To avoid the bulging of the PCB and the improper grounding due to the solder built up of the wires soldered in the bottom layer (Fig. 5.16), the base plate was milled i.e. material from the base plate was removed to form a rectangular slot as shown in Fig. 5.18. The solder built up will be positioned in the slot so that the bulging of the PCB is avoided.

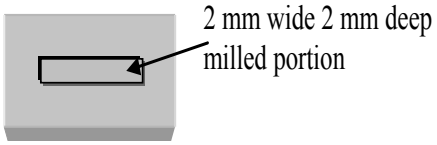



**Figure 5.18 Rectangular slot in the base plate.**

The circuit simulations done so far did not take the bends and T-junctions into account. One of the aspects of the microstrip behaviour is the evanescent modes around discontinuities arising due to abrupt change in the current direction. To include the discontinuity effects due to evanescent modes, the EM simulation was carried out for the bends and T-junction together. Fig. 5.19 shows the places where the bends and T-junctions were located for the circuit simulation. Fig. 5.20 shows the structure of the bends and T-junction together for the EM simulation. In the EM simulation setup the box size used was 20 mm x 20 mm and the cell size was 0.1 mm x 0.1 mm.

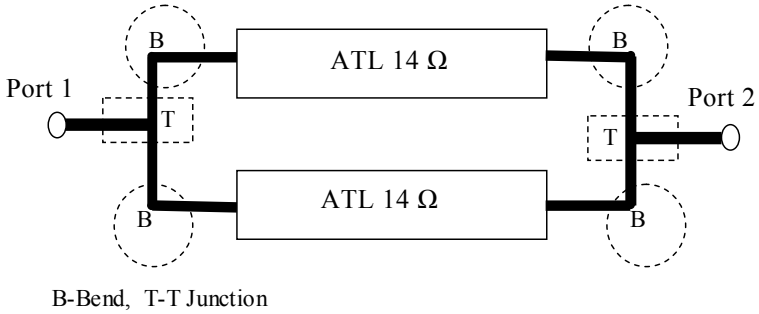



**Figure 5.19 Circuit simulation model with bends and T-junctions.**

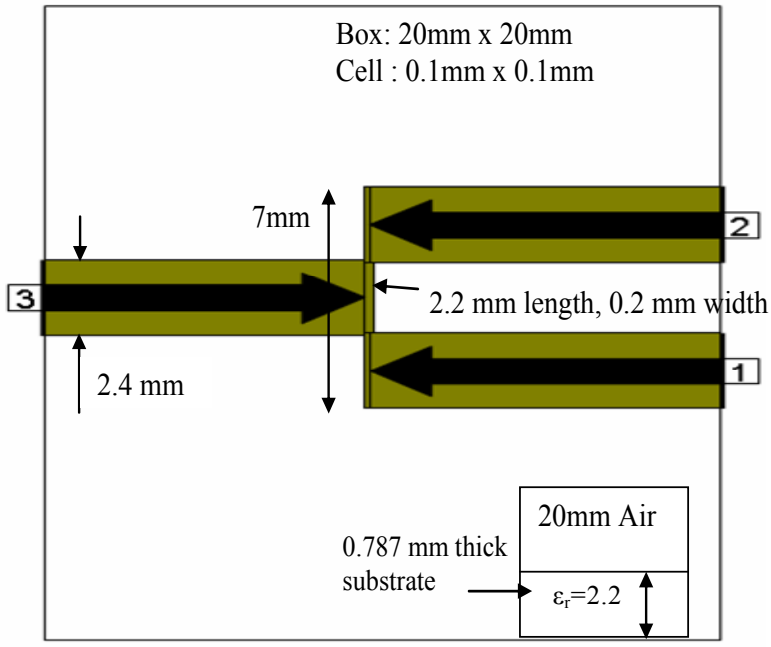



**Figure 5.20 EM simulation of the discontinuities in the evanescent modes.**

The EM simulated data was exported to the circuit simulation. Fig. 5.21 shows the schematic of the 7 Ω ATL with EM simulated bends and T-junctions. The circuit simulation S-parameter frequency responses are shown in Fig. 5.22.

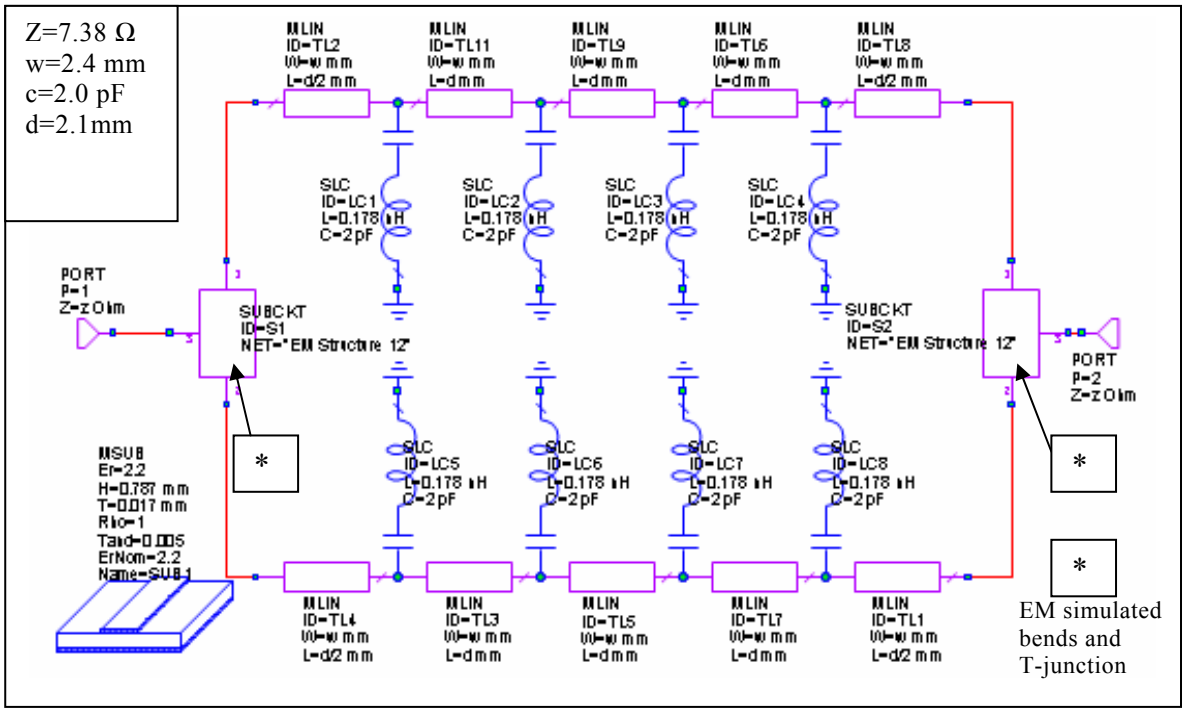



**Figure 5.21 7 Ω ATL schematic with EM simulated bends and T-junctions.**

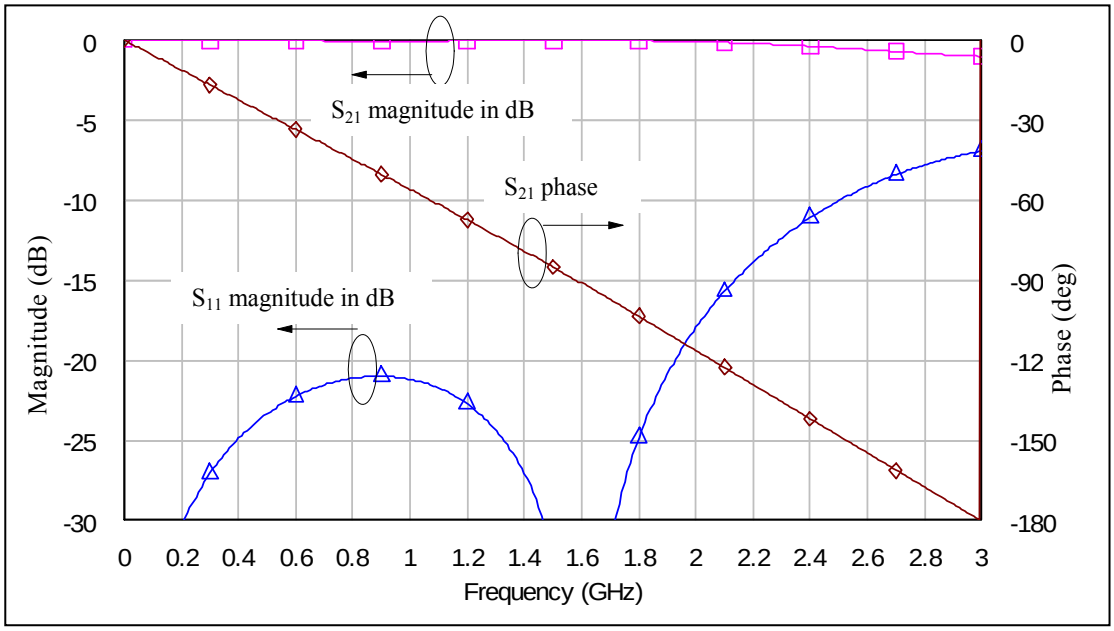



**Figure 5.22 Circuit simulated S-parameter responses of the 7 Ω ATL with EM simulated bends and T-junctions together (Port reference impedance = 7.38 Ω).**

The port impedances are tuned for minimum returnloss. The $S_{11}$ magnitude response in Fig. 5.22 shows that the ATL's characteristic impedance is close to the reference impedance 7.38 Ω.

### 5.3.2 EM Simulation of the 7 Ω ATL

During the circuit simulation, parasitic coupling effects between transmission lines were not taken into consideration. To account for the parasitic coupling effects the EM simulation of the 7 Ω ATL structure is required. The ATL structure for EM simulation is shown in Fig. 5.23. For the EM simulation the box size used was 50 mm x 40 mm and the cell size was 0.1 mm x 0.1 mm.

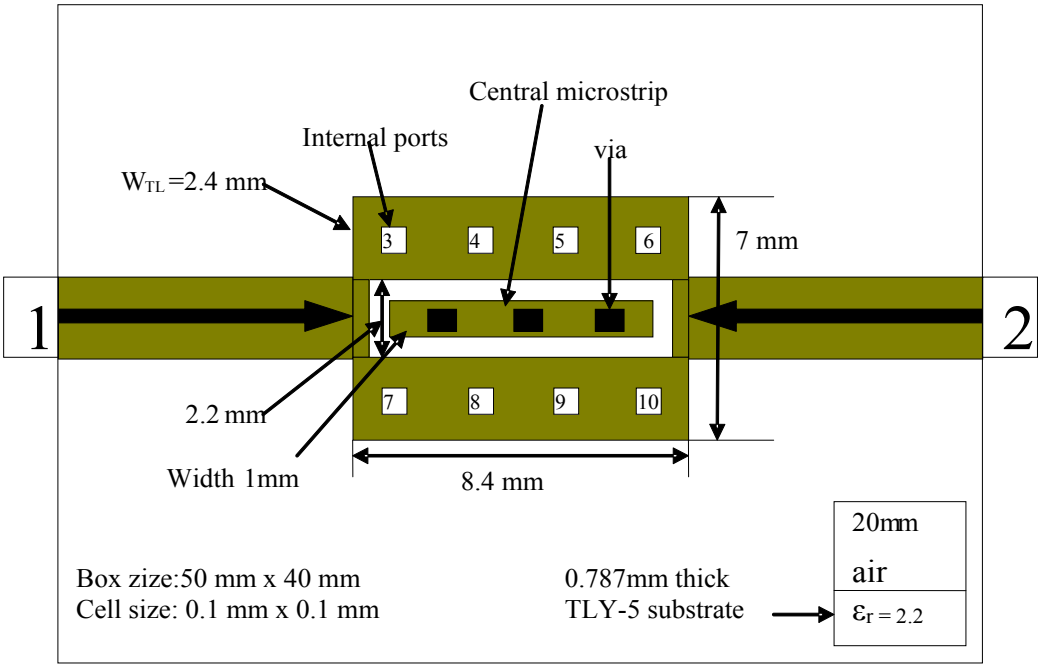



**Figure 5.23 EM simulation setup for the 7 Ω ATL structure.**

The box was closed in all directions. The EM simulation of the ATL geometry shown in Fig. 5.23 does not include the lumped capacitances. To include the shunt capacitances in the simulation, the EM simulated results of the ATL were made as a sub-circuit and exported to the circuit simulation. The internal ports in Fig. 5.23 are the places where the lumped capacitances will be connected in the circuit simulation.

The effects of the thin wire (inductance) used as a via for connecting the top and bottom layers of the PCB are required to be incorporated in the simulations. The dimensions of the wire were 0.8 mm diameter and 0.787 mm length (substrate thickness). To find out the inductance of the wire, the circuit simulation of the wire model as shown in Fig. 5.24 was carried out and the input impedance versus frequency response was plotted in Fig. 5.25. The input impedance (imaginary) of the wire at 2 GHz is 2.2 Ω and that corresponds to an inductance value of 180 pH.

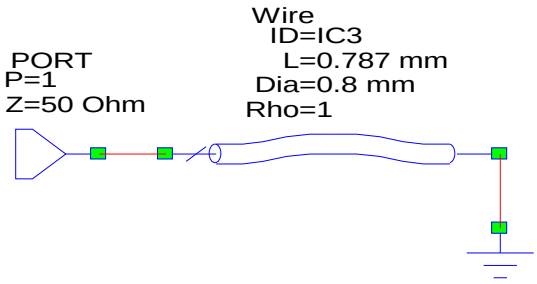



**Figure 5.24 Schematic of the wire (via) model.**

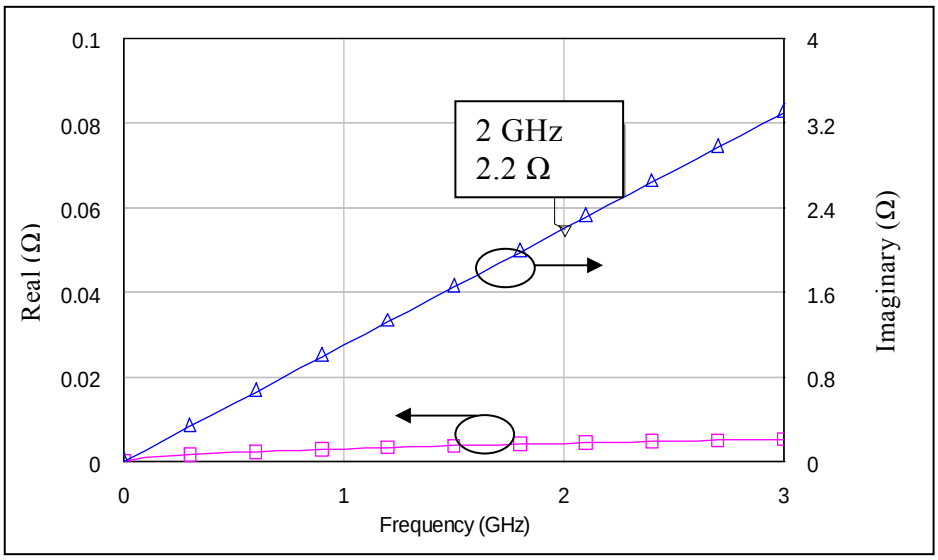



**Figure 5.25 Input impedance of the thin wire.**

The schematic for the circuit simulation with shunt capacitances and their parasitic inductances is shown in Fig. 5.26. The inductances (modelled) of the three wires used as vias were also included in the circuit simulation shown in Fig. 5.26. The port reference impedance Z was tuned until minimum returnloss was obtained. The circuit simulation results are shown in Fig. 5.27.

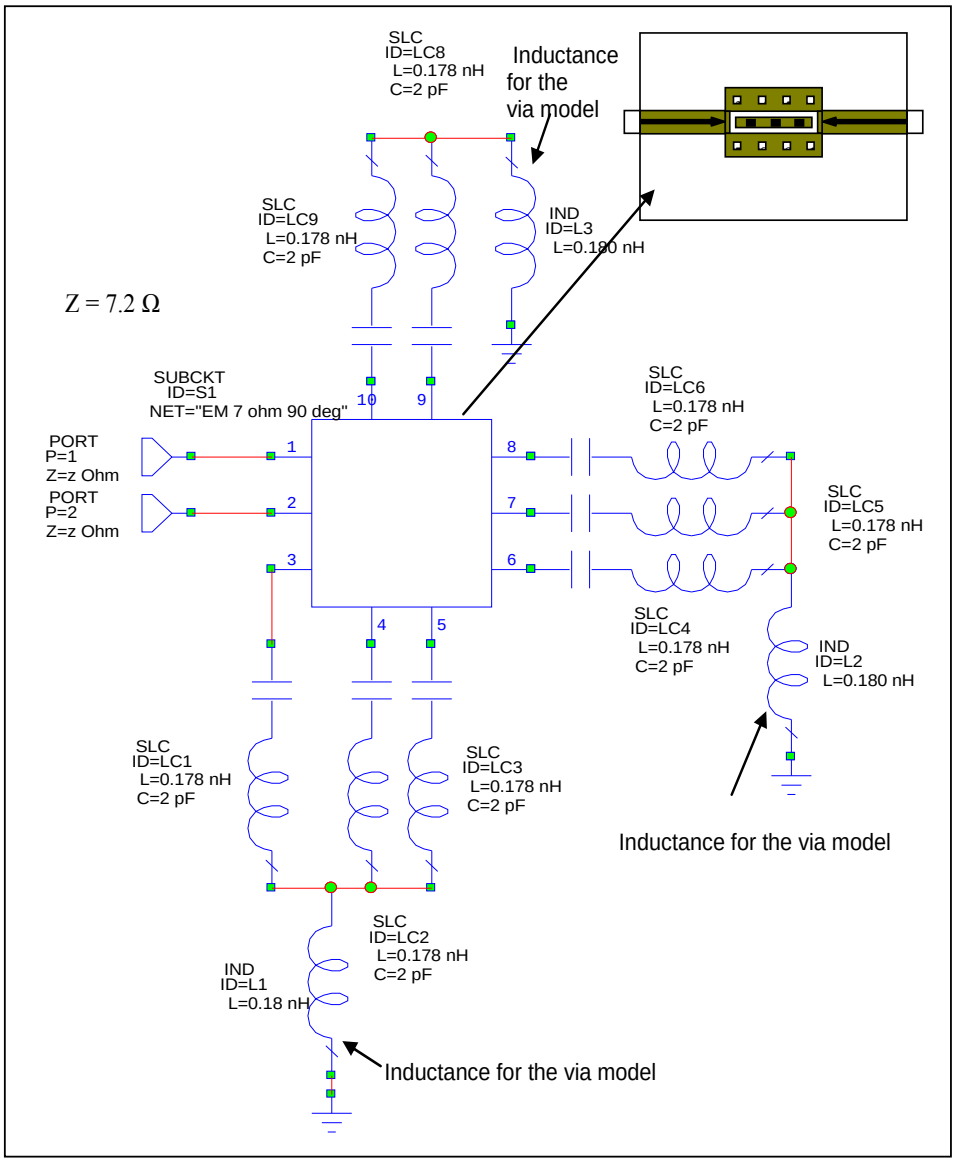



**Figure 5.26 Schematic of the 7 Ω ATL with EM simulated data, capacitors and via model.**

In Fig. 5.27, the minimum $S_{11}$ magnitude response was obtained with the reference impedance equal to 7.2 Ω meaning that the characteristic impedance of the ATL is 7.2 Ω. It can also be seen from Fig. 5.27 that the phase of the 7 Ω ATL is 90° at 1.7 GHz. A ripple around 2.3 GHz can also be seen in the $S_{11}$ and $S_{21}$ magnitude responses and also in the $S_{21}$ phase response. This may be due to the inductance of the via model (used for grounding). The S-parameter results of the circuit and EM simulations validate the design methods used for realising the 7 Ω ATL.

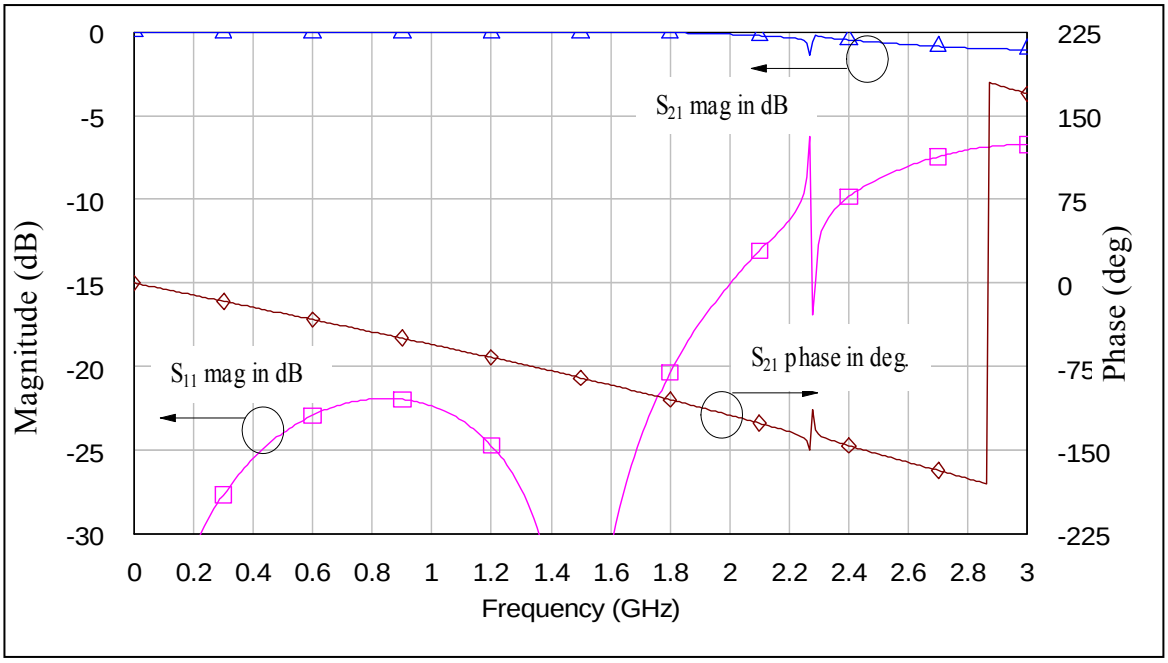



**Figure 5.27 EM simulated S-parameter responses of the 7 Ω ATL (Port reference impedance = 7.2 Ω).**

## 5.4 Experiment description and results

### 5.4.1 Layout

The layout was generated using MWO and then exported to CorelDRAW for adding mounting hole locations and the text. The photo of the assembled PCB with base plate is shown in Fig. 5.28. A 2.4 mm wide and 19 mm long microstrip (50 Ω) was connected at both ends of the ATL for soldering the SMA connectors.

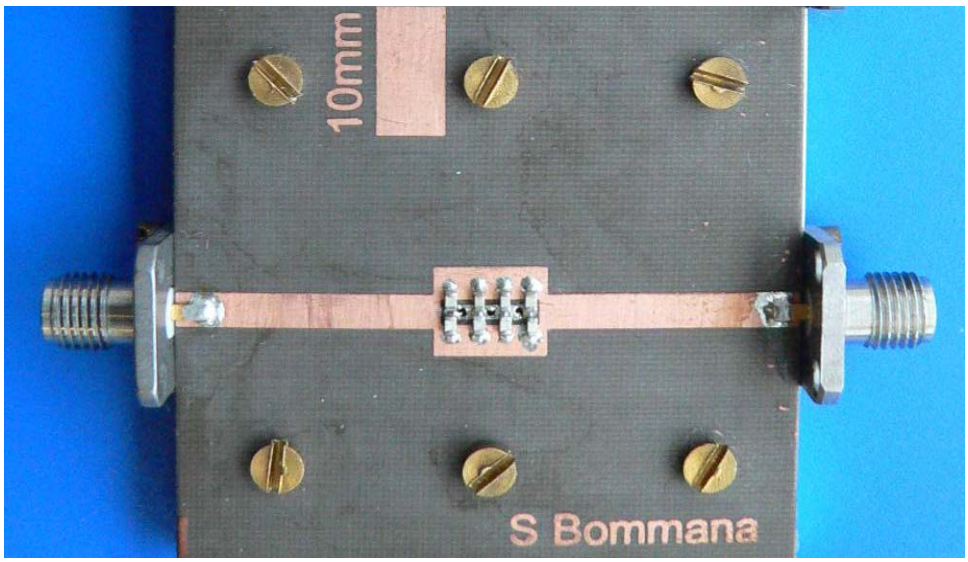
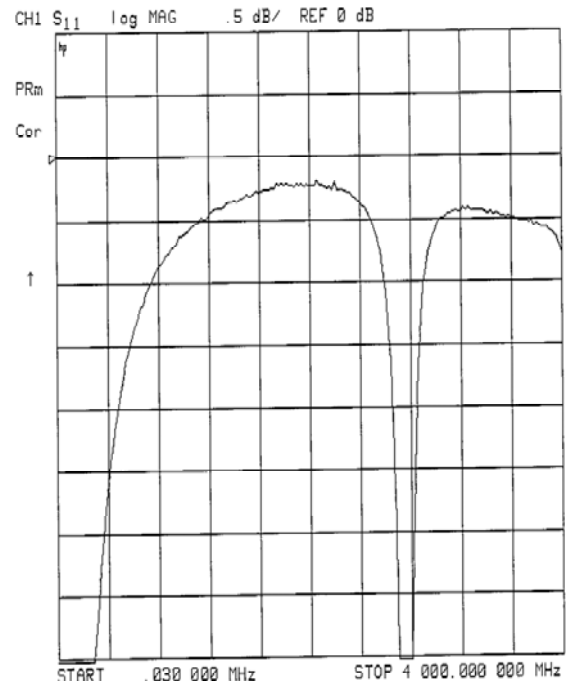



**Figure 5.28 Photo of the fabricated 7 Ω ATL.**

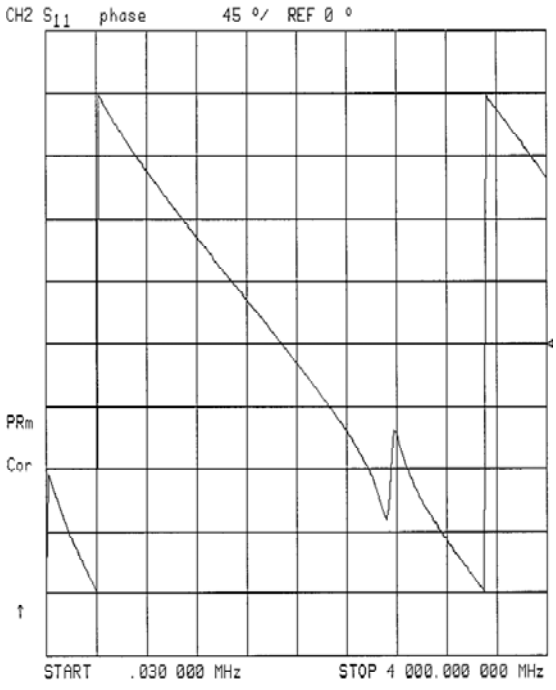
### 5.4.2 Measured results of the 7 Ω ATL

The measurements of the ATL were carried out with the HP8753D Vector Network Analyser. The VNA was calibrated (full two port) using a 3.5 mm calibration kit and then the measurements were taken. The Short-Open-Load-Thru (SOLT) calibration method was used. The male SMA connectors of the VNA test port cables were torqued using a torque spanner. Fig. 5.29 shows the raw S-parameter results. As the ATL is symmetric, only the $S_{11}$ magnitude and phase and $S_{21}$ magnitude and phase are shown.



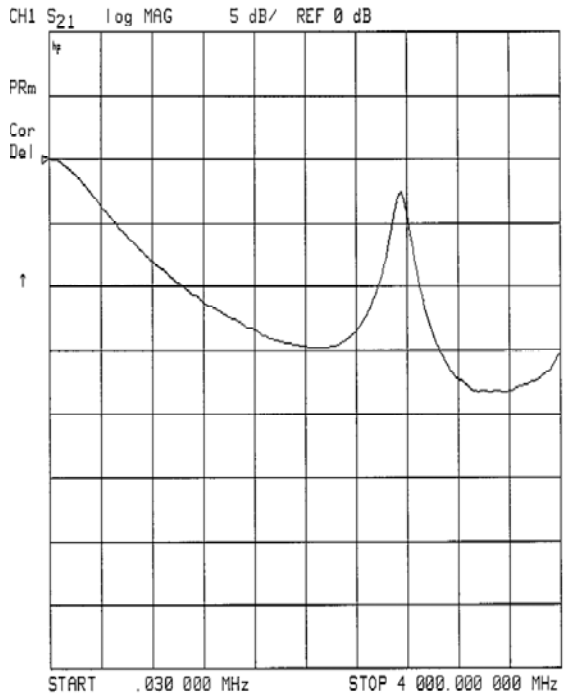

$S_{11}$ magnitude in dB

(a)



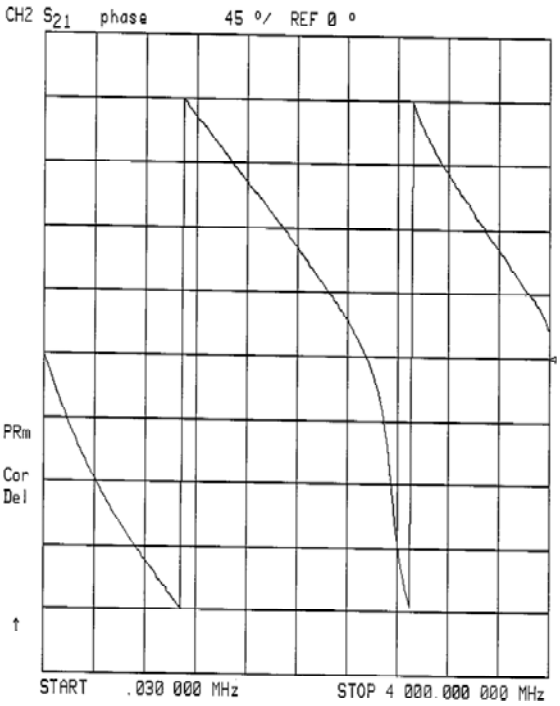

$S_{11}$ phase in deg

(b)




$S_{21}$ magnitude in dB

(c)




$S_{21}$ phase in degrees

(d)

**Figure 5.29 Raw measured S-parameter results of the 7 Ω ATL. (a) $S_{11}$ magnitude (dB). (b) $S_{11}$ phase (deg). (c) $S_{21}$ magnitude (dB). (d) $S_{21}$ phase (deg).**

### 5.4.3 De-embedding the measured data

The measured data includes the 50 Ω microstriplines connected to the ATL at both ends as shown in Fig. 5.30. DUT reference planes are also shown in Fig. 5.30.

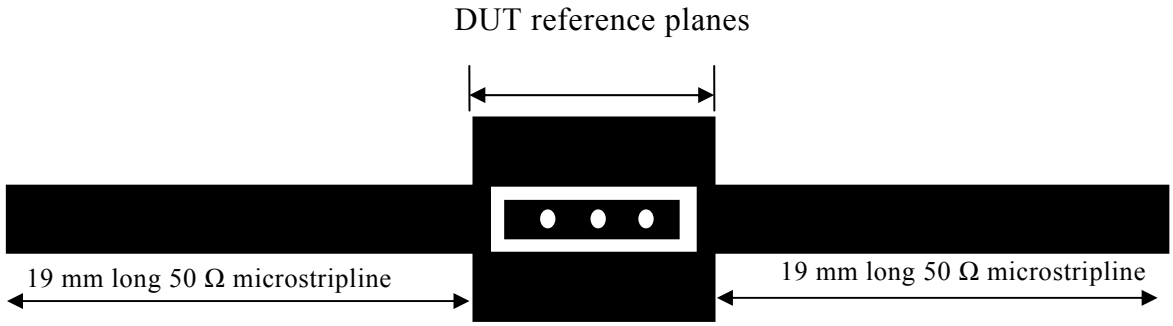



**Figure 5.30 7 Ω ATL reference planes.**

The 50 Ω microstriplines were de-embedded from the measured data to get the 7 Ω ATL results. The process of modelling the 50 Ω microstripline was explained in detail in Chapter 4. The values obtained for the SMA connector electrical length ($t$°) and the values of $L_1$, $C_1$ and $C_2$ (discontinuity model) in 50 Ω microstripline modelling were applied in the de-embedding of the 7 Ω ATL measured data. The electrical length of the 50 Ω microstrip connected at both ends of the ATL can be calculated as the physical length is known.

The schematic for the de-embedding of the 7 Ω ATL measured data is the same as the schematic used for the de-embedding of the 25 Ω ATL (Fig. 4.27). For the de-embedding of the 7 Ω ATL, the measured data in Fig. 4.27 is the measured data of the 7 Ω ATL and 19 mm long 50 Ω microstriplines are de-embedded in place of 15 mm long 50 Ω microstriplines. The data assignment for the de-embedding is shown in table 5.3. The reference impedance was tuned until minimum returnloss is obtained and the S-parameter responses of the de-embedded measurements are shown in Fig. 5.31.

| Data assignment for De-embedding | | |
|---|---|---|
| Measured data | | Raw data |
| $S_{11}$ | = | $S_{11}$ |
| $S_{21}$ | = | $S_{21}$ |
| $S_{12}$ | = | $S_{21}$ |
| $S_{22}$ | = | $S_{11}$ |

**Table 5.3 Data assignment for de-embedding the 7 Ω ATL measured data.**

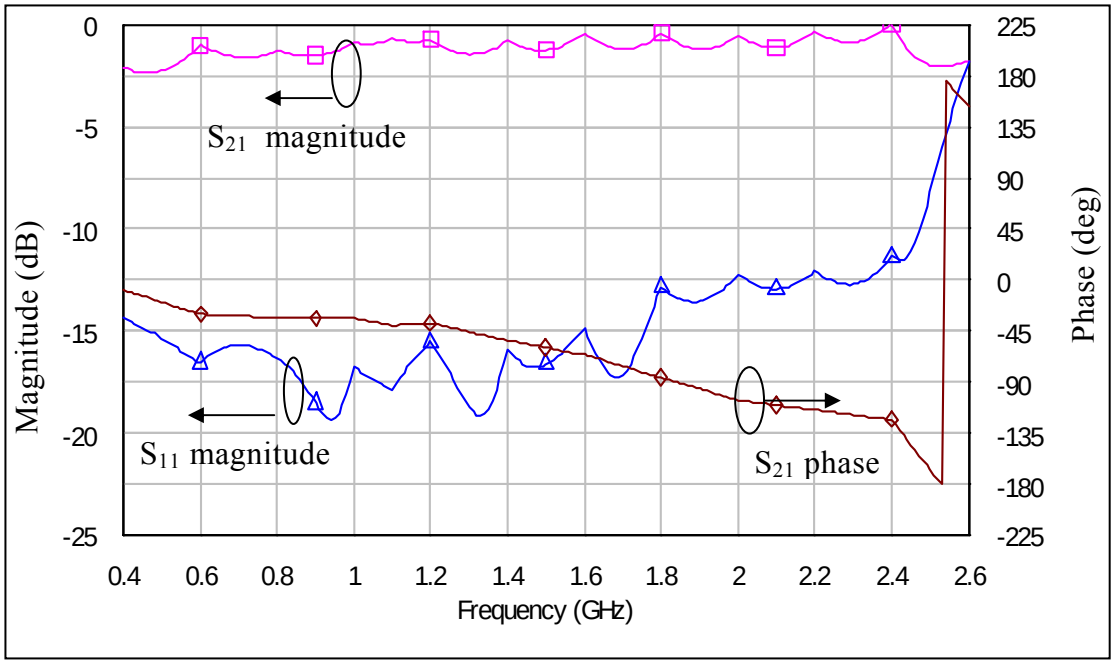



**Figure 5.31 De-embedded measured S-parameter responses of the 7 Ω ATL (Port reference impedance = 5.9 Ω).**

The tuned port reference impedance is 5.9 Ω, meaning the ATL characteristic impedance is 5.9 Ω. The phase of the ATL is 90° at 1.8 GHz. It can be concluded from the results of the circuit simulation, EM simulation and the de-embedded measured results that the design equations and the design method used in realising the 7 Ω ATL are valid.

# CHAPTER SIX

## ASYMMETRICAL POWER SPLITTER

### 6.1 Introduction

In this chapter the design and realisation of an asymmetrical power splitter is described. Different methods have been used in realising the asymmetrical power splitter [22-27] based on the Wilkinson power divider. In these papers the power splitter was realised by using one of the quarter-wavelength arms with high characteristic impedance transmission lines. In this project, the asymmetrical power splitter was realised by using the quarter-wavelength arms with the low impedance transmission lines. The design and fabrication of the 25 Ω and 7 Ω ATLs was described in Chapters 4 and 5 respectively and these two ATLs were used in realising the asymmetrical power splitter. The desired centre frequency of the asymmetrical power splitter was 2 GHz. The theory of the asymmetrical power splitter is given in section 6.2. In section 6.3, the design of a 25 Ω ATL with 90° phase is described and in section 6.4, details of the simulation of the asymmetrical power splitter is given. Sections 6.5 and 6.6 describe the experimental description and the measured results and the de-embedded measured results of the asymmetrical power splitter.

### 6.2 Theory

The block diagram of an asymmetrical power splitter based on the Wilkinson power splitter is shown in Fig. 6.1. The power splitter has two quarter-wavelength arms with the characteristic impedances $Z_{o2}$ and $Z_{o3}$ and was terminated with the reference

impedance $Z_o$. $Z_{in2}$ is the input impedance of the quarter-wave transmission line with the characteristic impedance $Z_{o2}$ and $Z_{in3}$ is the input impedance of the quarter-wave transmission line with the characteristic impedance $Z_{o3}$; $Z_{in2}$ is not equal to $Z_{in3}$. $P_{in}$ is the power at the input port and the $P_2$ and $P_3$ are the powers delivered to the terminations at the output ports. $V_1$ is the voltage at the input port. There is an input quarter-wavelength transmission line (Fig. 6.1) with the characteristic impedance of $Z_{o1}$. The input quarter-wave transmission line was terminated with the reference impedance $Z_o$ at the input side.

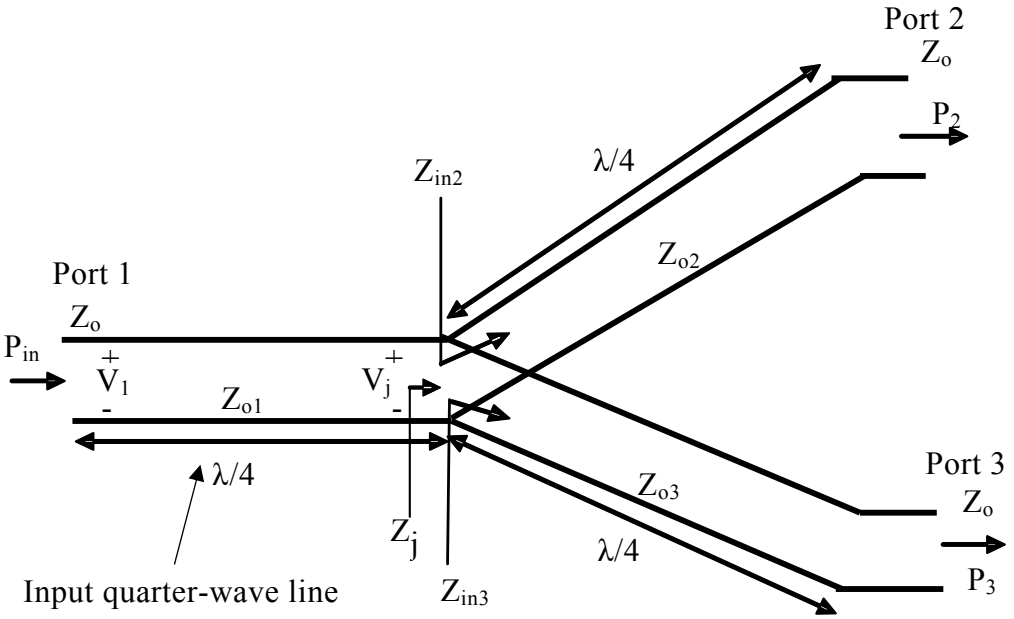



**Figure 6.1 An asymmetrical power splitter.**

The quarter-wave transmission line behaves as an impedance transformer and the characteristic impedance of a quarter-wave transformer will be equal to square root of the input and output impedances. The input impedance $Z_{in2}$ can be written as:

$$Z_{in2} = \frac{Z_{o2}^{\ 2}}{Z_o} . \qquad (47)$$

Similarly,

$$Z_{in3} = \frac{Z_{o3}^{\ 2}}{Z_o} . \tag{48}$$

If the input impedance of the two quarter-wave transmission lines is $Z_j$ then,

$$Z_j = \frac{Z_{in2} Z_{in3}}{Z_{in2} + Z_{in3}} . \tag{49}$$

$Z_j$ is the load for the input quarter-wave transmission line and if the input is matched to $Z_o$ then,

$$Z_{o1} = \sqrt{Z_j Z_o} . \tag{50}$$

Since $P_{in}$ is the input power to the power splitter,

$$P_{in} = \frac{V_1^2}{2Z_o} . \tag{51}$$

As the quarter-wave transmission lines are lossless, the input power $P_{in}$ is delivered to $Z_j$. If $V_j$ is the voltage at $Z_j$ then,

$$V_j = \sqrt{2P_{in} Z_j} . \tag{52}$$

Since $V_j$ is the voltage at the junction of the three quarter-wave transmission lines, power delivered to port 2 termination,

$$P_2 = \frac{V_j^{\ 2}}{2Z_{in2}} . \tag{53}$$

Substituting (47) in (53):

$$P_2 = \frac{V_j^2}{2\left(\frac{Z_{o2}^2}{Z_o}\right)}. \tag{54}$$

Similarly power delivered to port 3 termination,

$$P_3 = \frac{V_j^2}{2\left(\frac{Z_{o3}^2}{Z_o}\right)}. \tag{55}$$

From (54) and (55),

$$\frac{P_2}{P_3} = \frac{Z_{o3}^2}{Z_{o2}^2}. \tag{56}$$

Therefore for a power splitter shown in Fig. 6.1, the output power split ratio is inversely proportional to the square of the individual characteristic impedances of the quarter-wavelength arms.

In this project the reference impedance was 50 Ω and the two quarter-wavelength arms characteristic impedances were 25 Ω and 7 Ω. The input impedance of the 7 Ω quarter-wave arm can be calculated using (47) and is equal to 1 Ω. Similarly for the 25 Ω quarter-wave arm the input impedance can be calculated using (48) and is equal to 12.5 Ω. The input impedance $Z_j$ can be calculated using (49) and is equal to 0.9 Ω.

The input quarter-wave transmission line is required to match the load impedance of 0.9 Ω to 50 Ω. The characteristic impedance of the input quarter-wave transmission line, $Z_{o1} = \sqrt{50 \times 0.9}$ = 6.7 Ω. As the characteristic impedance of the input quarter-wave

transmission line is very close to 7 Ω, the 7 Ω ATL was used for the input quarter-wave transmission line. Since $Z_{o1}$ is equal to $Z_{o2}$, $S_{32}$ will be equal to $S_{31}$.

## 6.3 25 Ω ATL with 90° phase length

In Chapter 4, a 25 Ω ATL with an electrical length of 180° at 2 GHz was realised. To realise a 25 Ω ATL with 90° electrical length at 2 GHz the ATL structure was cut into two halves; each half will be of quarter-wavelength. Fig. 6.2 shows the ATL structure of the 25 Ω ATL with the electrical length of 90° at 2 GHz.

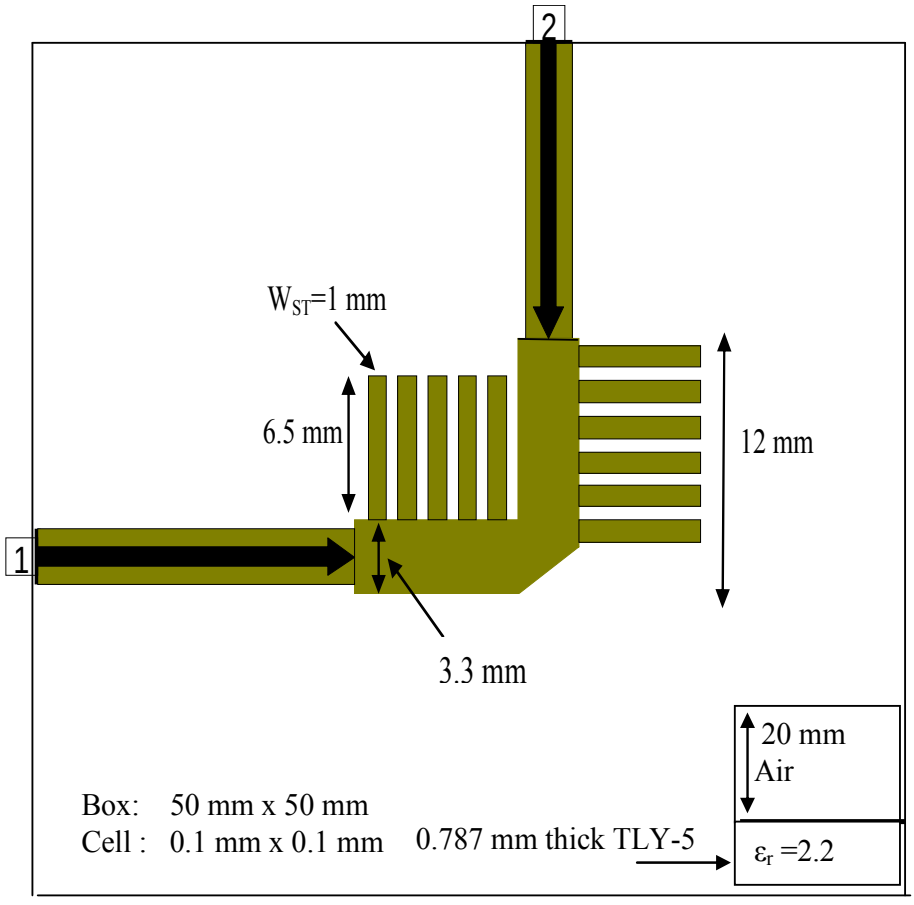



**Figure 6.2 EM simulation setup for the 25 Ω ATL structure with 90° electrical length at 2 GHz.**

An EM simulation was carried on the structure shown in Fig. 6.2. The box size was 50 mm x 50 mm and the cell size was 0.1 mm x 0.1 mm. To determine the ATL's

characteristic impedance, the port impedances were tuned until the minimum $S_{11}$ (magnitude) was obtained. Fig. 6.3 shows the S-parameter results of the 25 Ω ATL with the port impedance tuned to 25.1 Ω. The magnitude response of $S_{11}$ indicates that the characteristic impedance of the ATL is close to the reference impedance and that means the characteristic impedance of the ATL is 25.1 Ω. From the $S_{21}$ phase response it can be seen that the phase of the ATL is 90° at 1.9 GHz.

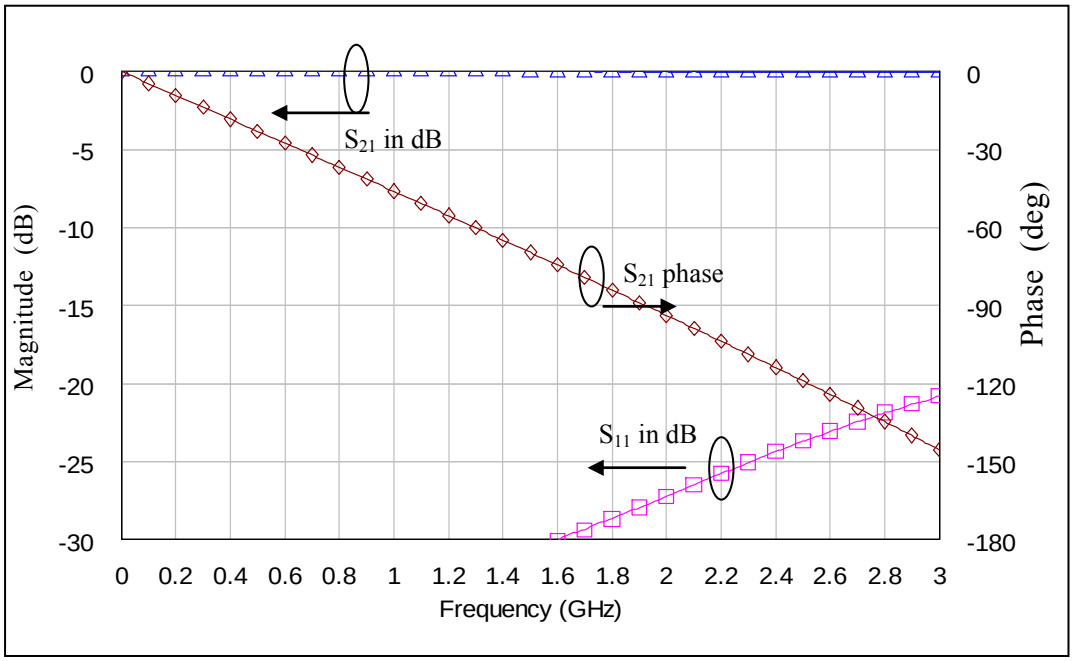
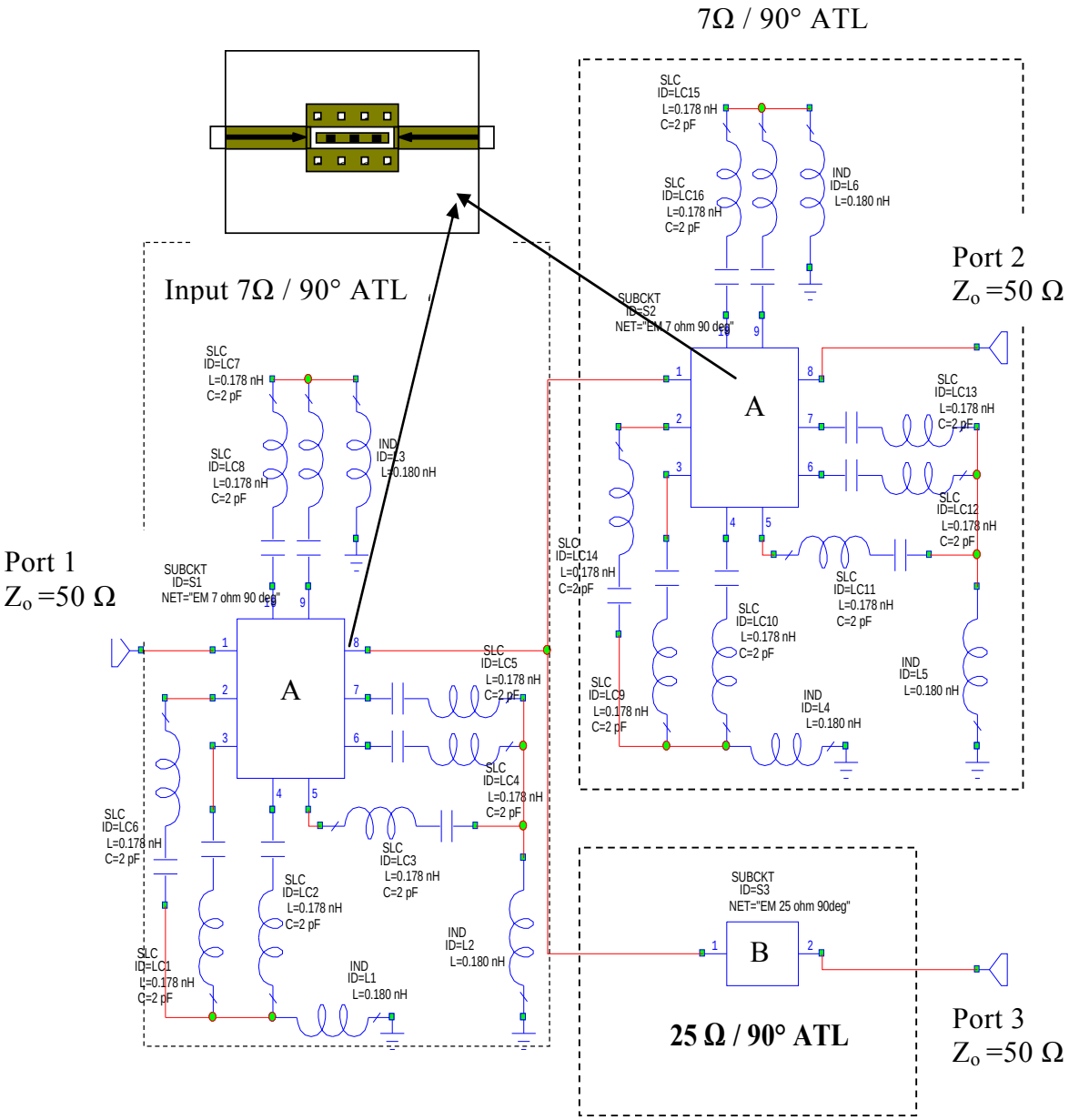



**Figure 6.3 EM simulated S-parameter responses of the 25 Ω ATL with 90° electrical length at 1.9 GHz (Port reference impedance = 25.1 Ω).**

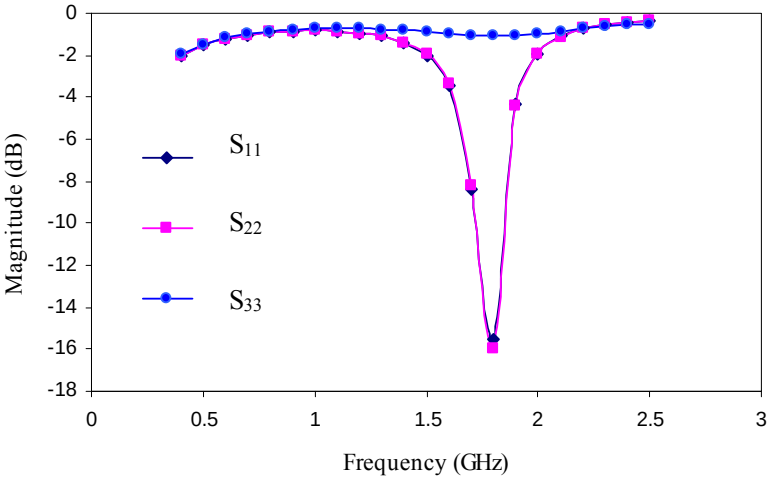
## 6.4 Simulation of the asymmetrical power splitter

Fig. 6.4 shows the schematic of the asymmetrical power splitter. The asymmetrical power splitter consists of an input matching quarter-wave transmission line and two quarter-wavelength arms. The characteristic impedances of the two quarter-wavelength arms of the asymmetrical power splitter are 25.1 Ω and 7.2 Ω which results in a power split ratio of 10.8 dB. All the three ports are terminated with 50 Ω. The circuit simulated S-parameter results are shown in Fig. 6.5.

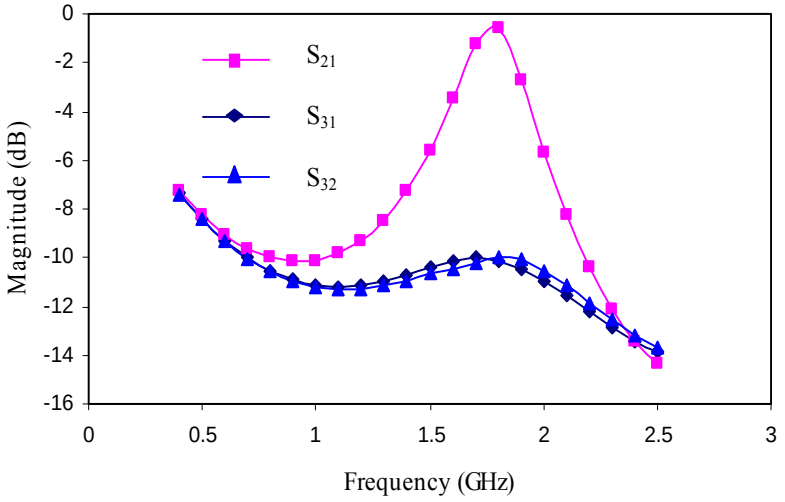



A: EM structure of the 7 Ω ATL  B: EM structure of the 25 Ω ATL

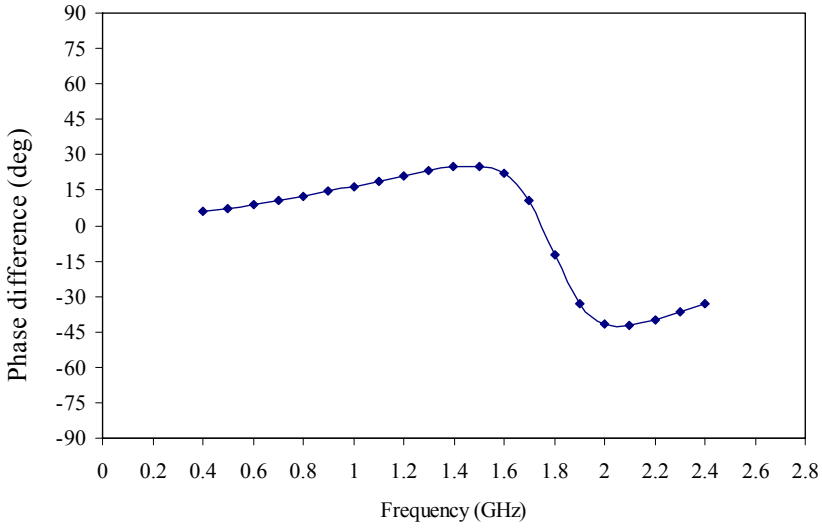
**Figure 6.4 Schematic of the asymmetrical power splitter.**




(a)




(b)




(c)

**Figure 6.5 Circuit simulated S-parameter responses of the asymmetrical power splitter (Port reference impedance = 50 Ω). (a) Magnitudes of $S_{11}$, $S_{22}$ and $S_{33}$ in dB. (b) Magnitudes of $S_{21}$, $S_{31}$ and $S_{32}$ in dB. (c) Phase difference of $S_{21}$ and $S_{31}$ in degrees.**

From Fig. 6.5 (b), the power divider split ratio can be found from the magnitudes of $S_{21}$ and $S_{31}$ which is equal to 10.1 dB at the centre frequency of 1.8 GHz. From Fig. 6.5 (c), it can be observed that the phase difference between $S_{21}$ and $S_{31}$ is very small at the centre frequency as required. It can also be seen that the magnitudes of $S_{31}$ and $S_{32}$ are equal. From Fig. 6.5 (a), the magnitude responses of $S_{11}$ and $S_{22}$ show that the input port and port 2 of the power divider are well matched to 50 Ω at the centre frequency. The $S_{33}$ (magnitude) result shows that port 3 is not well matched to 50 Ω. The parallel connection of the 7 Ω quarter-wave lines (Fig. 6.1) means that the input impedance seen by the 25 Ω quarter-wave arm is

$$= \frac{7^2}{50} \left\| \frac{7^2}{50} \right. = 0.49\ \Omega.$$

Port 3 input impedance = $\frac{25^2}{0.49} = 1275\,\Omega.$

So, $$\left|S_{33}\right| = 0.924$$

$$\approx -0.69\,dB,$$

and hence port 3 is highly mismatched.

## 6.5 Experimental description

The layout of the asymmetrical power splitter is shown in Fig. 6.6. The layout was generated using MWO and exported to CorelDRAW for adding text and mounting hole locators. The 50 Ω microstriplines of 19 mm length were added at the input and the output ports of the asymmetrical power splitter for soldering the SMA connectors. A separate 7 Ω ATL was also added in the layout for characterising the ATL. The experimental results of the 7 Ω ATL were discussed in Chapter 5.

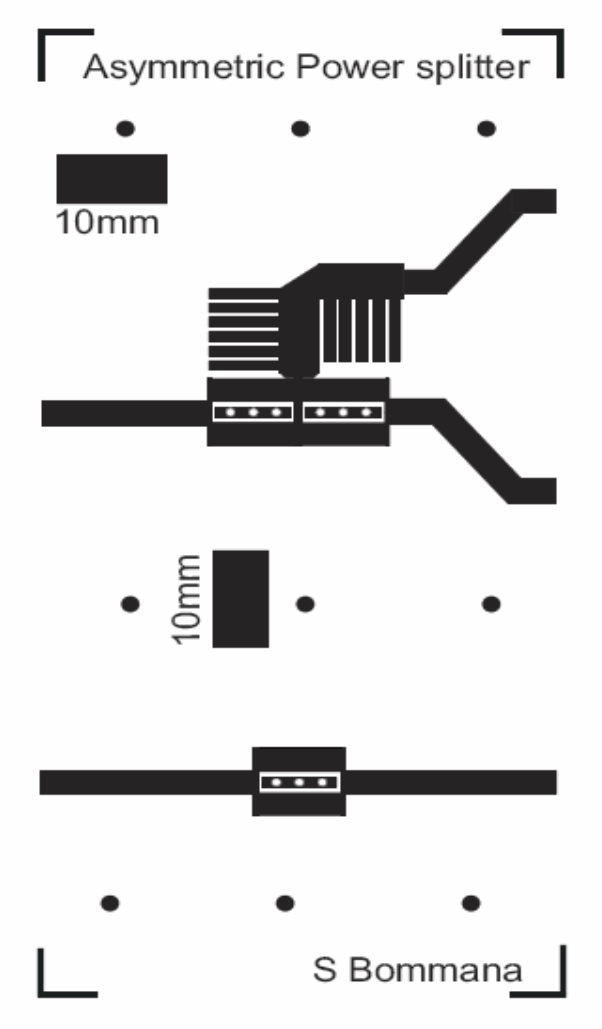



**Figure 6.6 Layout of the Power splitter along with the 7 Ω ATL.**

A double sided PCB was fabricated using Taconic TLY-5 substrate. The PCB was fastened to an aluminium base plate using screws. The screws were sufficiently spaced from the ATL and the power splitter to avoid any coupling of the screws with the printed circuits. The SMA connectors were fastened to the base plate using the screws and the centre pins of the SMA connectors were soldered to the ports of the power splitter. Fig. 6.7 shows the photo of the assembled PCB and the SMA connectors mounted on the base plate.

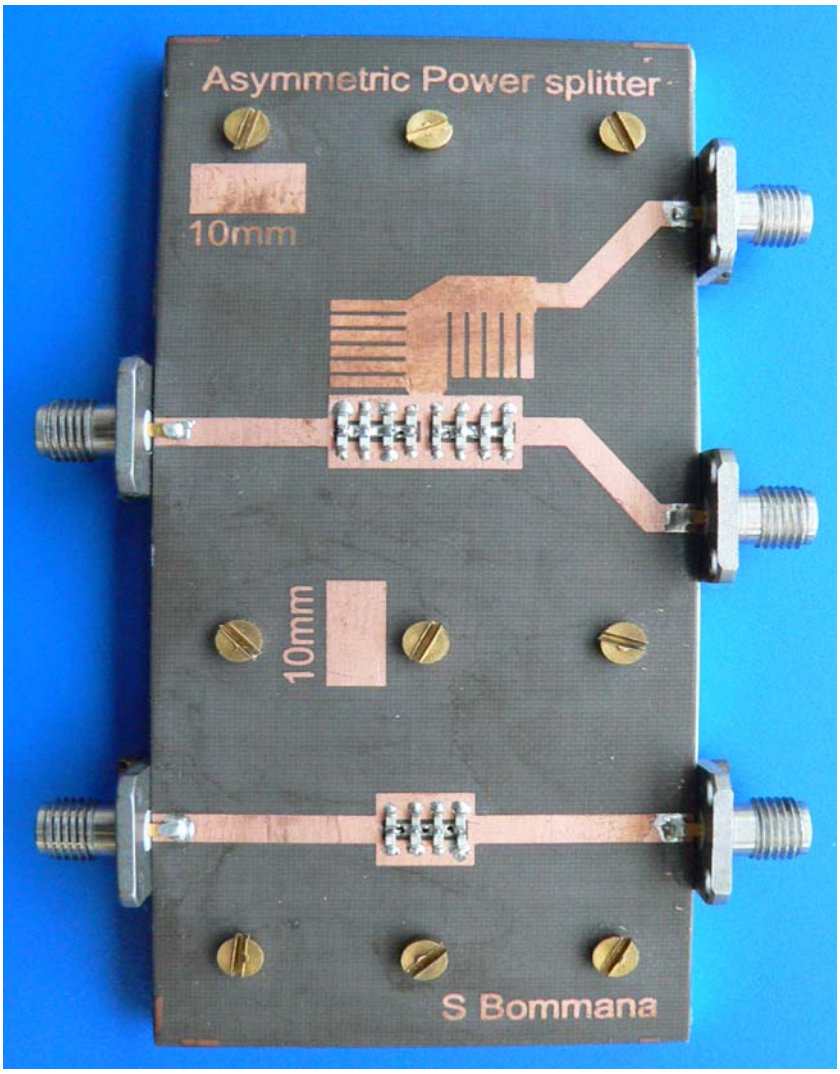



**Figure 6.7 Photo of the fabricated asymmetrical power splitter along with the 7 Ω ATL.**

## 6.6 Measured results

The S-parameter responses of the power splitter were measured using the HP8753D Vector Network Analyser. The VNA was calibrated (full two port) using a 3.5 mm calibration kit prior to taking the measurements. The Short-Open-Load-Thru (SOLT) calibration method was used. The male SMA connectors of the VNA test port cables were torqued using a torque spanner.

### 6.6.1 Measurement setup 1

As the power splitter has 3 ports, two sets of measurements were taken. The first set of measurements was taken with port 3 terminated with 50 Ω as shown in Fig. 6.8. The measurement results are shown in Fig. 6.9.

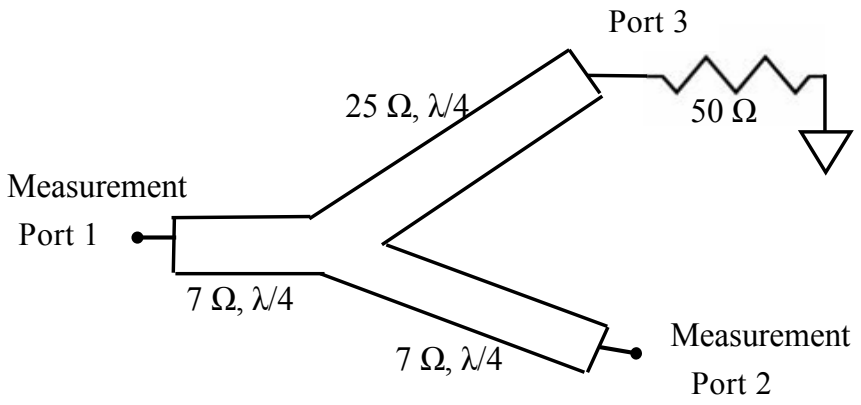
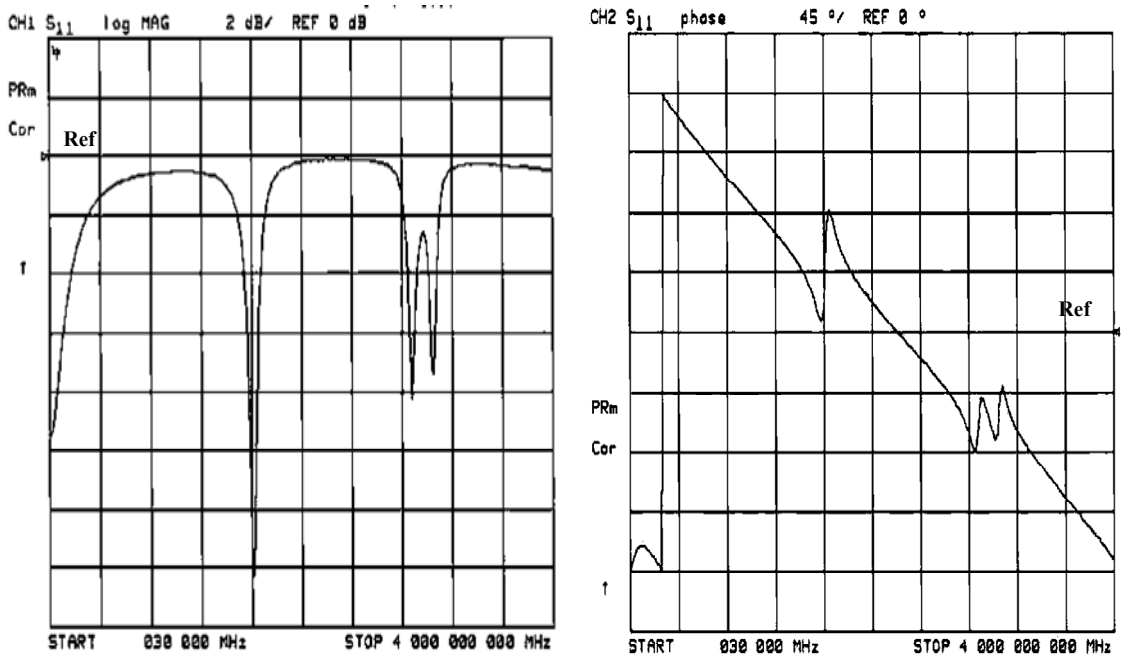
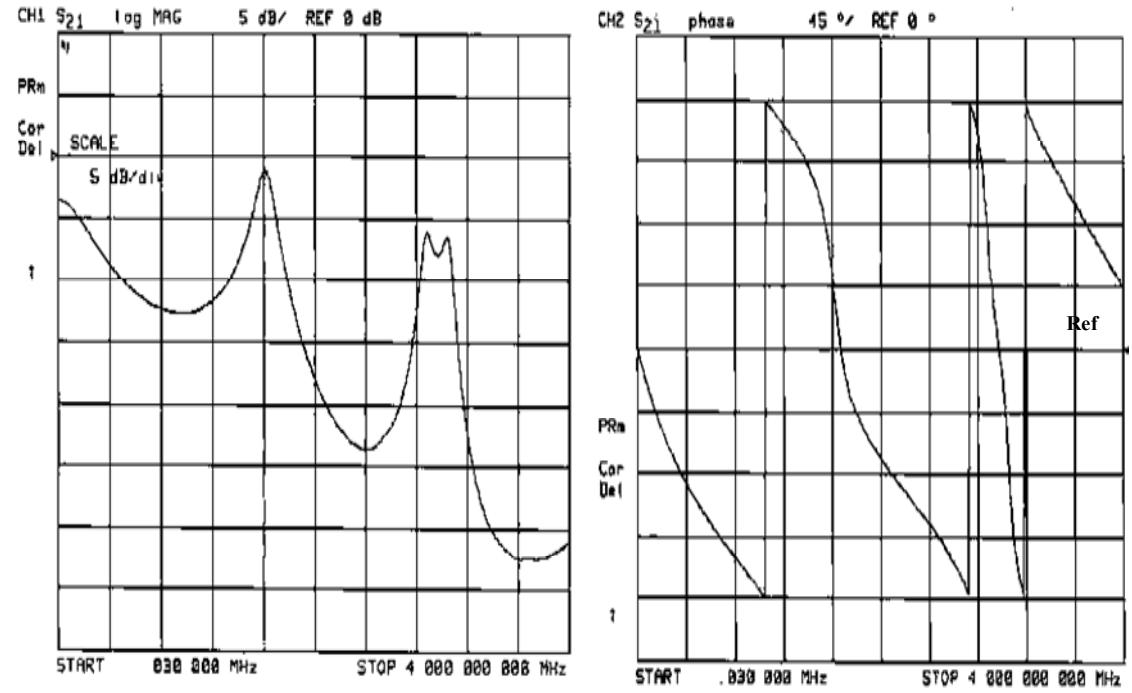


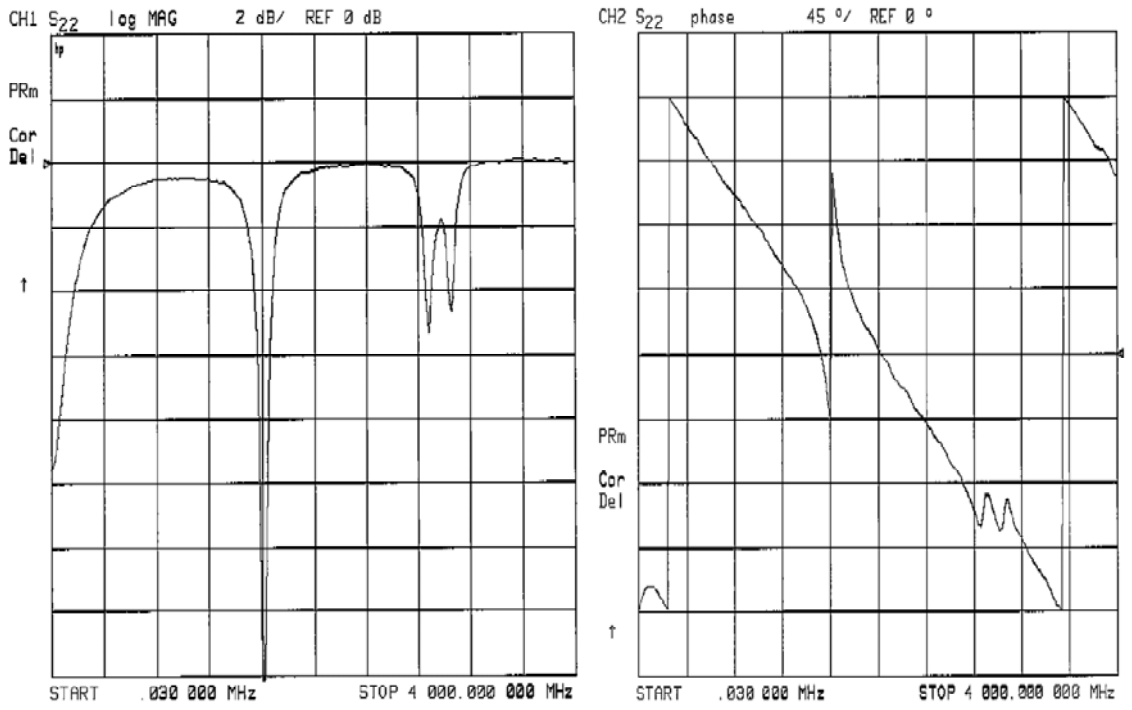

**Figure 6.8 Power splitter measurement setup 1.**




**(a)**




**(b)**




**(c)**

**Figure 6.9 Raw measured S-parameter responses of the power splitter (setup 1). (a) $S_{11}$ magnitude and phase. (b) $S_{21}$ magnitude and phase. (c) $S_{22}$ magnitude and phase.**

### 6.6.2 Measurement setup 2

The second set of measurements was taken with port 2 terminated with 50 Ω as shown in Fig. 6.10. The measurement results are shown in Fig. 6.11.

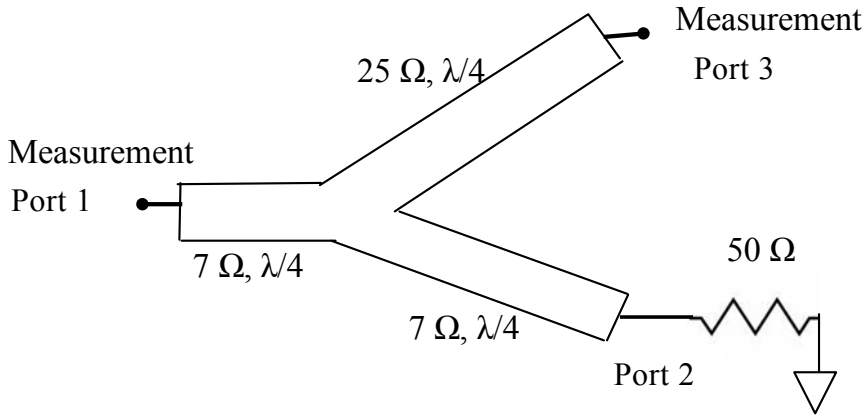
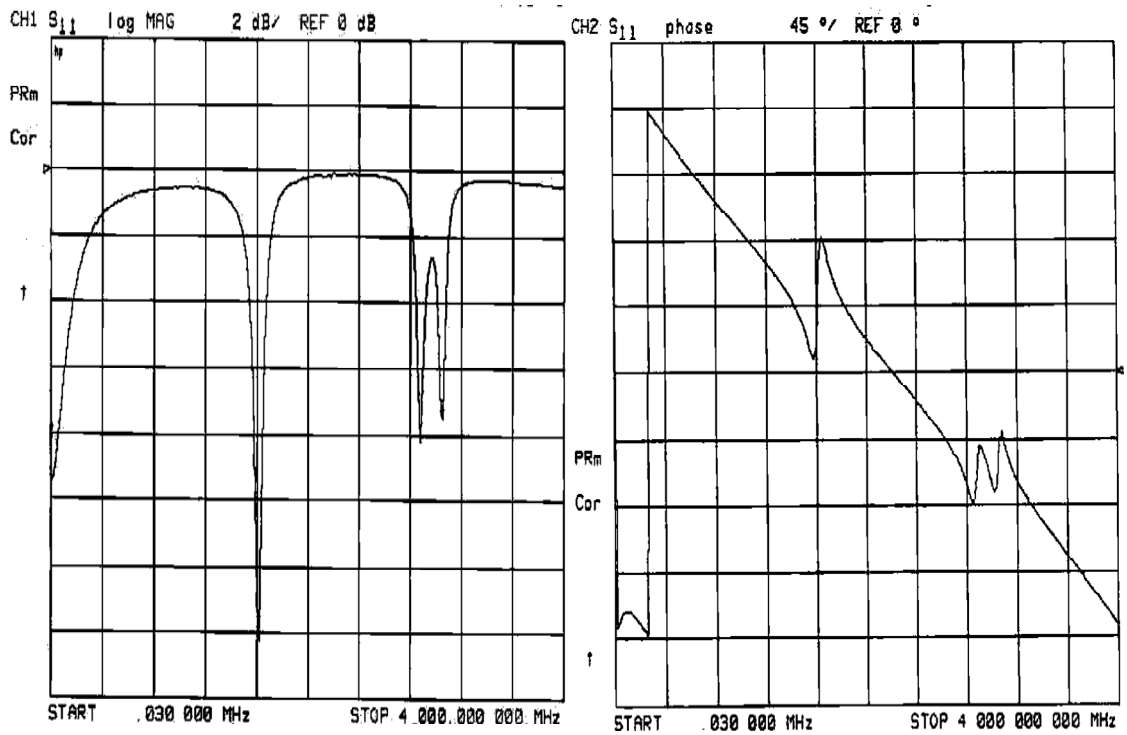
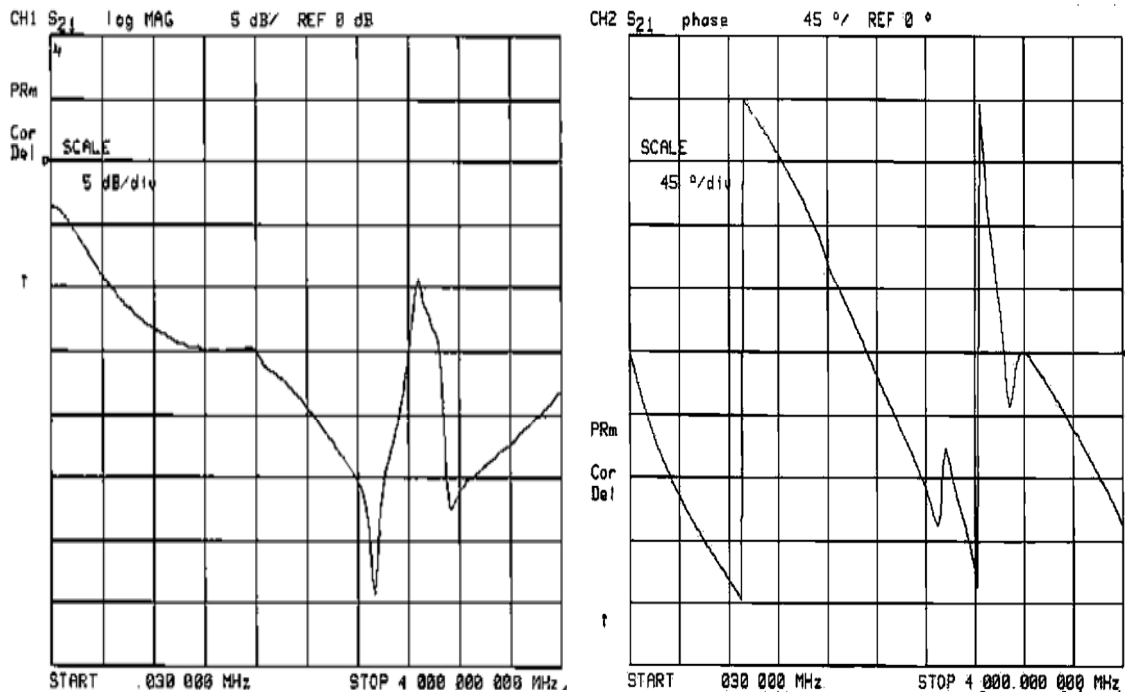


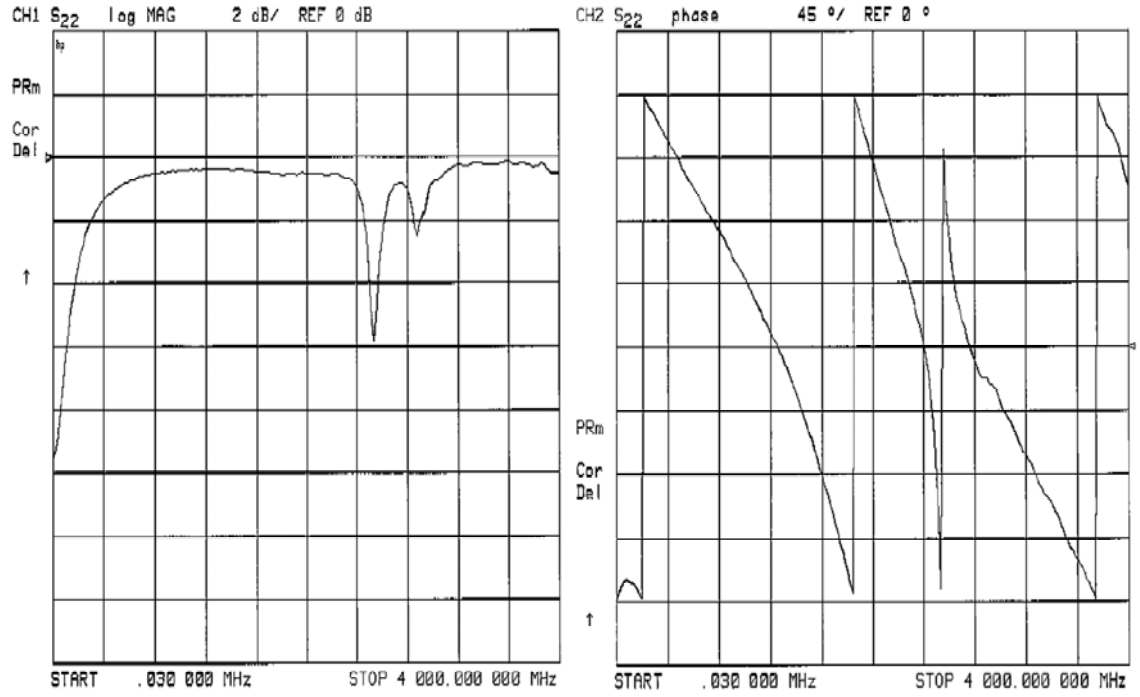

**Figure 6.10 Power splitter measurement setup 2.**




**(a)**




**(b)**




**(c)**

**Figure 6.11 Raw measured S-parameter responses of the power splitter (setup 2). (a) $S_{11}$ magnitude and phase. (b) $S_{21}$ magnitude and phase. (c) $S_{22}$ magnitude and phase.**

### 6.6.3 De-embedded measured data

The measurements were taken with the additional 50 Ω microstriplines added to the asymmetrical power splitter for connecting the SMA connectors. To obtain the results of the power splitter, it is necessary to remove the 50 Ω microstripline lengths and the discontinuity effects of the SMA connector. The process of modelling the 50 Ω microstripline was explained in detail in Chapter 4. The values obtained for the SMA connector electrical length (t°) and the values of $L_1$, $C_1$ and $C_2$ (discontinuity model) in the 50 Ω microstripline modelling were applied in de-embedding the power splitter measured data.

The de-embedding method is explained in Chapter 4. The schematic for de-embedding the power splitter measured data is same as the schematic shown in Fig. 4.27. The measured data in Fig. 4.27 was replaced with the measured data of the power splitter and 19 mm long 50 Ω microstriplines were de-embedded in place of 15 mm long 50 Ω microstriplines. To get the power splitter output power split ratio the de-embedding was applied to the measured data from the measurement setups 1 and 2. The data assignment for the de-embedding is shown in the table 6.1.

| Data assignment for the de-embedding | | |
|---|---|---|
| Measured data | | Raw data |
| $S_{11}$ | = | $S_{11}$ |
| $S_{21}$ | = | $S_{21}$ |
| $S_{12}$ | = | $S_{21}$ |
| $S_{22}$ | = | $S_{22}$ |

**Table 6.1 Data assignment for the de-embedding of the measured data of the power splitter.**

The S-parameter plots of the de-embedded measured results are shown in Fig. 6.12. The de-embedded results of the $S_{21}$ and $S_{22}$ from the measurement setup 2 will become $S_{31}$ and $S_{33}$.

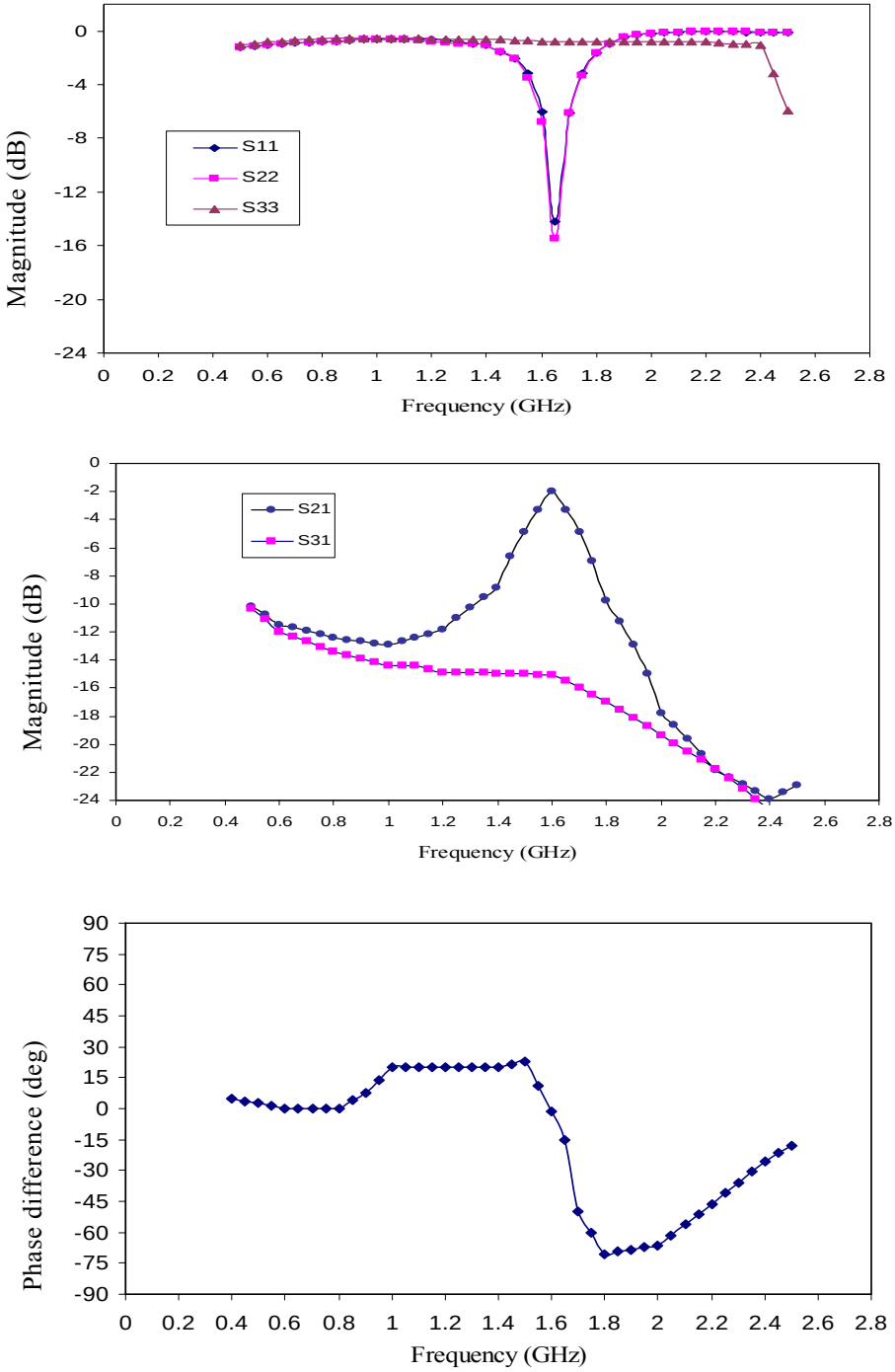



**Figure 6.12 De-embedded measured S-parameter responses of the power splitter (Port reference impedance = 50 Ω). (a) Magnitudes of $S_{11}$, $S_{22}$ and $S_{33}$ in dB. (b) Magnitudes of $S_{21}$ and $S_{31}$ in dB. (c) Phase difference of $S_{21}$ and $S_{31}$ in degrees.**

The magnitudes of $S_{11,}$ $S_{22}$ and $S_{33}$ are plotted in Fig. 6.12 (a). The magnitudes of $S_{21}$ and $S_{31}$ are plotted in Fig. 6.12 (b) and Fig. 6.12 (c) shows the plot of phase difference between $S_{21}$ and $S_{31}$ in degrees. The ratio of magnitudes (dB) of $S_{21}$ and $S_{31}$ gives the power splitter output power split ratio.

From the de-embedded measured results shown in Fig 6.12, the centre frequency of the power splitter is 1.60 GHz. At the centre frequency the phase difference between $S_{21}$ and $S_{31}$ will be zero. The shift in the centre frequency from the desired centre frequency (2 GHz) may be due to the junction discontinuities between the three ATLs (7 Ω ATLs and 25 Ω ATL).

The magnitude plots of $S_{11}$ and $S_{22}$ in Fig. 6.12 (a) show that the input port (Port 1) and port 2 are well matched to 50 Ω at the centre frequency. The magnitude results of $S_{33}$ show that port 3 is not matched to 50 Ω. In section 6.4, detailed description was given on why port 3 is not matched to 50 Ω.

The magnitudes of $S_{21}$ and $S_{31}$ are plotted in Fig. 6.12 (b). From the de-embedded measured results, the power split ratio is 13 dB at the centre frequency of 1.60 GHz. A power splitter with 25 Ω ATL and 7 Ω ATL as the quarter-wave arms should have the power split ratio of about 11 dB which is different from the measured de-embedded power split ratio. From the de-embedded measured results (Fig. 5.31) of the 7 Ω ATL, the characteristic impedance of the ATL is 5.9 Ω and from the de-embedded measured results (Fig. 4.31) of the 25 Ω ATL, the characteristic impedance of the ATL is 24.4 Ω. The power split ratio calculated using these two characteristic impedances is 12.4 dB which is very close to the measured de-embedded power split ratio of 13 dB.

The phase difference of $S_{21}$ and $S_{31}$ is plotted in Fig. 6.12 (c). The phase difference between $S_{21}$ and $S_{31}$ is very small at the centre frequency of 1.60 GHz suggesting that the electrical length between port 1 and port 2 and port 1 and port 3 is same as required.

The results of the power splitter depend on the characteristic impedances of the ATLs that are used and the frequency at which the ATLs will be of quarter-wavelength. The other important element is the input matching transformer and in this project to ease the realisation of the power splitter a 7 Ω ATL was used though the required $Z_o$ of the matching transformer was different. Though the results are slightly offset from the desired results, this project work demonstrates that an asymmetrical power splitter can successfully be constructed using the low impedance ATLs and reasonably good results can be obtained.

# CHAPTER SEVEN

## CONCLUSIONS

The demand for miniaturisation of the electronic circuits is the prime motivation for the design and realisation of the low impedance transmission lines and the asymmetrical power splitter. A transmission line with characteristic impedance of as low as 7 Ω at 1.8 GHz was designed and realised in this project. A 25 Ω transmission line at 2.1 GHz was also realised. The 7 Ω and 25 Ω transmission lines were realised based on the ATL concept and using the design equations [12]. The ATLs were realised on a PCB with a substrate thickness of 0.787 mm and dielectric constant of 2.2. An asymmetrical power splitter was realised using the 7 Ω ATL and the 25 Ω ATL as the quarter-wave arms.

The circuit and EM simulations were carried out for the design and realisation of the ATLs and the asymmetrical power splitter. Microwave Office was used for the circuit and EM simulations. The raw measured results of the ATLs and the asymmetrical power splitter were de-embedded to get the device measured results.

The 25 Ω ATL was realised using microstriplines only, where as microstriplines and chip capacitors were used in realising the 7 Ω ATL. The measured characteristic impedance of the realised 25 Ω ATL was 24.4 Ω and the measured electrical length was 180° at 2.1 GHz. A meandered microstripline ($\varepsilon_r$ = 2.2, $h$ = 0.787 mm) with characteristic impedance of 25 Ω and electrical length of 180° at 2 GHz will have a size of 34 mm x 15 mm. In this project the 25 Ω ATL with 180° electrical length at 2.1 GHz was realised in a size of 22 mm x 19 mm. The design of the 25 Ω ATL resulted in 18% reduction in area compared to the meandered microstripline.

It was also shown in this project that the spacing between the adjacent lines can be less than 3 times the substrate thickness, and 0.6 mm spacing was used between adjacent stubs to realise a compact ATL structure. Meandering and space-filling techniques were used to achieve a compact size for the 25 Ω ATL.

A conventional microstripline with characteristic impedance of 7 Ω and electrical length of 90° at 1.8 GHz will have a size of about 28 mm x 27 mm ($\varepsilon_r$ = 2.2, $h$ = 0.787 mm). Such a wide (27 mm) microstripline may not behave as a transmission line. In this project it was shown that the 7 Ω ATL with 90° electrical length at 1.8 GHz can be realised within a size of 7 mm x 8.4 mm which is only 8% of the conventional 7 Ω microstripline area. The measured characteristic impedance of the realised 7 Ω ATL was 5.9 Ω and the ATL was 90° at 1.8 GHz. Though the measured results were slightly offset from the specifications, the goal of this project work was primarily to verify the feasibility and implementation of the low impedance transmission lines using the ATL concept and the measured results prove that the goal was achieved.

The measured results of the power splitter show that the centre frequency of the power splitter was 1.6 GHz. At the centre frequency the phase difference between $S_{21}$ and $S_{31}$ will be zero. The shift in the centre frequency from the specification of 2 GHz may be attributed to the junction discontinuities. The measured power split ratio was 13 dB which is different from the desired power split ratio of 11 dB. The difference in power split ratio can be attributed to the measured characteristic impedances of the ATLs which were 24.4 Ω and 5.9 Ω. The power split ratio calculated using these two characteristic impedances will be 12.4 dB which is very close to the measured power split ratio.

To conclude, the contributions of the thesis include: design and realisation of a low impedance transmission line with characteristic impedance as low as 5.9 Ω and electrical length of 90° at 1.8 GHz using the ATL concept; realisation of an asymmetrical power splitter with the output power split ratio of 13 dB using the 5.9 Ω and 24.4 Ω ATLs as the quarter-wavelength arms.

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# APPENDIX 1

## SUBSTRATE DATA SHEET

TLY

Dimensionally Stable
Low Loss
Low Moisture Absorption
High Peel Strength
Uniform & Consistent DK

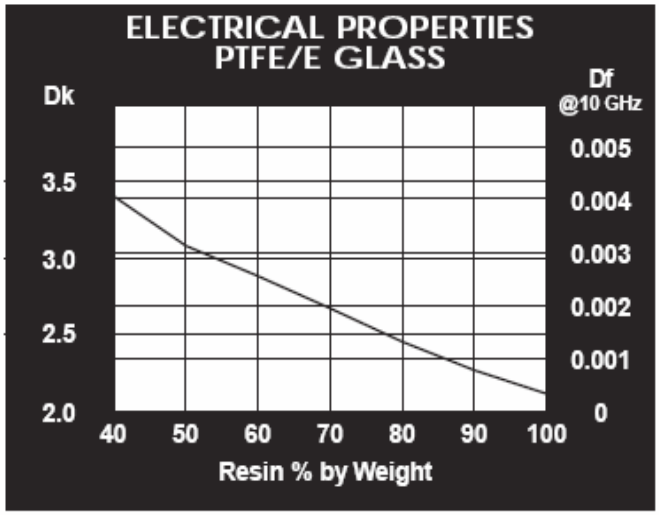
Mullingar Business Park
Mullingar, Co. Westmeath,
Republic of Ireland
TEL: +353-44-95600
FAX: +353-44-44369

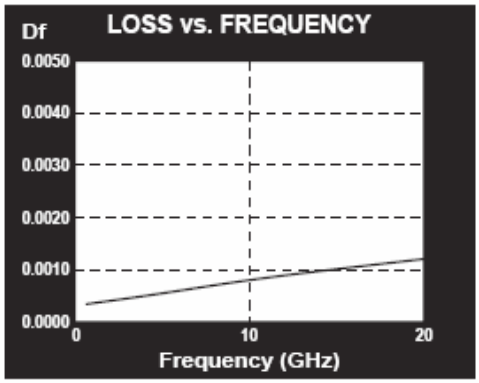
TACONIC
P.O. Box 69 • 136 Coonbrook Road
Petersburgh, NY 12138
TEL: 518-658-3202 • FAX: 518-658-3988
TOLL FREE: 800-833-1805 • FAX: 800-272-2503

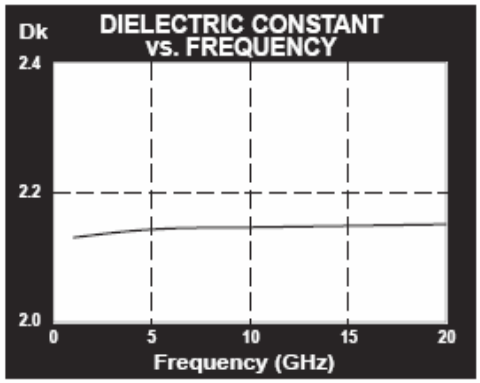
702 Se-Sung Plaza
366-4 Yatap-dong Bundang-ku
Sungnam-si, Kyungki-do
Republic of Korea
TEL: 82-31-704-1858/9
FAX: 82-31-704-1857

| TLY-5 TYPICAL VALUES | | | | | |
|---|---|---|---|---|---|
| Property | Test Method | Units | Value | Units | Value |
| Dielectric Constant @ 10 GHz | IPC-TM 650 2.5.5.5 | | 2.20 | | 2.20 |
| Dissipation Factor @ 10 GHz | IPC-TM 650 2.5.5.5 | | 0.0009 | | 0.0009 |
| Moisture Absorption | IPC-TM 650 2.6.2.1 | % | <0.02 | % | <0.02 |
| Dielectric Breakdown | IPC-TM 650 2.5.6 | kV | >60 | kV | >60 |
| Volume Resistivity | IPC-TM 650 2.5.17.1 | Mohm/cm | $10^7$ | Mohm/cm | $10^7$ |
| Surface Resistivity | IPC-TM 650 2.5.17.1 | Mohm | $10^7$ | Mohm | $10^7$ |
| Arc Resistance | IPC-TM 650 2.5.1 | seconds | >180 | seconds | >180 |
| Flexural Strength Lengthwise | IPC-TM 650 2.4.4 | lbs./in. | >12,000 | N/mm² | >83 |
| Flexural Strength Crosswise | IPC-TM 650 2.4.4 | lbs./in. | >10,000 | N/mm² | >69 |
| Peel Strength (1oz copper) | IPC-TM 650 2.4.8 | lbs./linear in. | 12.0 | N/mm | 2.1 |
| Thermal Conductivity | ASTM F 433 | W/m/K | 0.22 | W/m/K | 0.22 |
| x-y CTE | ASTM D 3386 (TMA) | ppm/°C | 20 | ppm/°C | 20 |
| z CTE | ASTM D 3386 (TMA) | ppm/°C | 280 | ppm/°C | 280 |
| UL-94 Flammability Rating | UL-94 | | V-0 | | V-0 |

| Type | Dk |
|---|---|
| TLY-5A | 2.17 |
| TLY-5 | 2.20 |
| TLY-3 | 2.33 |
| TLT-0 \| TLX-0 | 2.45 |
| TLT-9 \| TLX-9 | 2.50 |
| TLT-8 \| TLX-8 | 2.55 |
| TLT-7 \| TLX-7 | 2.60 |
| TLT-6 \| TLX-6 | 2.65 |
| TLE-95 | 2.95 |
| TLC-27 | 2.75 |
| TLC-30 | 3.00 |
| TLC-32 | 3.20 |
| RF-30 | 3.00 |
| RF-35 \| RF-35P | 3.50 |
| RF-60 | 6.15 |
| CER-10 | 10 |



# APPENDIX 2

## ATC 600S SERIES CHIP CAPACITOR DATA SHEET

### ATC 600S Series
### Ultra-Low ESR, High Q, NPO
### RF & Microwave Capacitors

**Features:**

- **Lowest ESR in Class**
- Highest Working Voltage in class – 250V
- Standard EIA Size: 0603
- Laser Marking (Optional)
- High Self Resonance Frequencies

**Applications:**

- Cellular Base Stations
- Wireless Commuications
- Broadband Wireless Services
- Satellite Communications
- WiMAX (802.16)

**Circuit Applications:**

- Filter Networks
- High Q Frequency Sources
- Matching Networks
- Tuning, Coupling, Bypass and DC Blocking

**ATC 600 SERIES OVERVIEW**

| ATC Series | ATC Case Size | EIA Case Size |
|---|---|---|
| 600 | L | 0402 |
| **600** | **S** | **0603** |
| 600 | F | 0805 |

**Electrical Specifications**

| | |
|---|---|
| **Capacitance:** | 0.1 to 100 pF |
| **Tolerances:** | See Cap Value Chart |
| **Working Voltage (WVDC):** | 250 V |
| **Quality Factor (Q):** | ≥ 2000 |
| **Operating Temperature Range:** | -55°C too +125°C (no derating of working voltage) |
| **Temperature coefficient of Capacitance (TCC):** | 0 ± 30 ppm/°C, -55°C to +125° |
| **Insulation Resistance:** | $10^5$ MΩ min. at +25°C at rated WVDC<br>$10^4$ MΩ min. at +125°C at rated WVDC |
| **Dielectric Withstanding Voltage (DWV):** | 2.5 x WVDC for 5 seconds |
| **Aging:** | None |
| **Piezo Effects:** | None |

**Mechanical Specifications**

| | |
|---|---|
| **Terminations:** | T = Tin Plated over Nickel Barrier* (Standard)<br>W = Tin/Lead Solder Plated over Nickel Barrier |
| **Solderability:** | Solder coverage > 90% of end termination |
| **Terminal Strength:** | 4 lbs. Typ., 2 lbs. min. |

**Environmental Specifications**

| | |
|---|---|
| **Life Test:** | 2000 hours, +125°C at 2X WVDC |
| **Thermal Shock:** | 5 cycles, -55°C to +125°C |
| **Moisture Resistance:** | 240 hours, 85% Relative Humidity at +85°C |

**Military Approval**

DSCC Drawing Number 05002

**RoHS Compliant*

ATC 600 Series Capacitors are designed and manufactured to meet and exceed the requirements of EIA-198, MIL-PRF-55681 and MIL-PRF-123.

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ISO 9001 REGISTERED COMPANY

THE ENGINEERS' CHOICE™

ATC 001-924; Rev. M 4/07

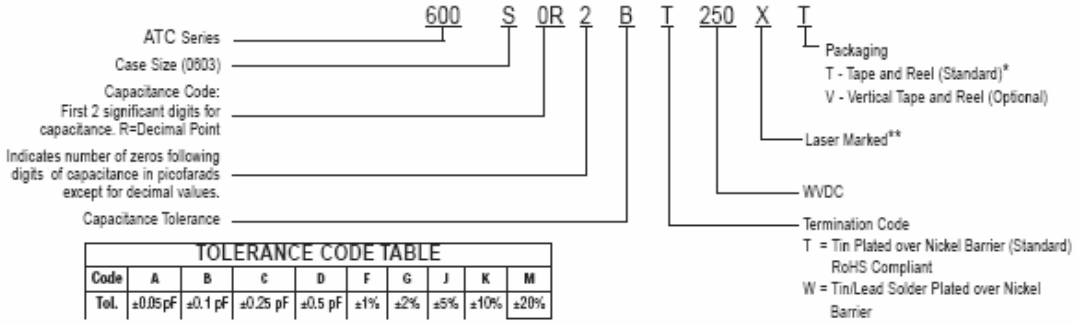
# ATC 600S Series Ultra-Low ESR, High Q NPO RF & Microwave Capacitors

## Capacitance Values

| Value (pF) | Cap Code | Marking | Tolerances | Value (pF) | Cap Code | Marking | Tolerances | Value (pF) | Cap Code | Marking | Tolerances |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.1 | 0R1 | A9 | A, B | 2.7 | 2R7 | L0 | A, B, C, D | 20 | 200 | H1 | F, G, J, K, M |
| 0.2 | 0R2 | H9 | A, B | 3.0 | 3R0 | M0 | A, B, C, D | 22 | 220 | J1 | F, G, J, K, M |
| 0.3 | 0R3 | M9 | A, B, C | 3.3 | 3R3 | N0 | A, B, C, D | 24 | 240 | K1 | F, G, J, K, M |
| 0.4 | 0R4 | d9 | A, B, C | 3.6 | 3R6 | P0 | A, B, C, D | 27 | 270 | L1 | F, G, J, K, M |
| 0.5 | 0R5 | f9 | A, B, C | 3.9 | 3R9 | Q0 | A, B, C, D | 30 | 300 | M1 | F, G, J, K, M |
| 0.6 | 0R6 | m9 | A, B, C | 4.3 | 4R3 | R0 | A, B, C, D | 33 | 330 | N1 | F, G, J, K, M |
| 0.7 | 0R7 | n9 | A, B, C | 4.7 | 4R7 | S0 | A, B, C, D | 36 | 360 | P1 | F, G, J, K, M |
| 0.8 | 0R8 | t9 | A, B, C | 5.1 | 5R1 | T0 | A, B, C, D | 39 | 390 | Q1 | F, G, J, K, M |
| 0.9 | 0R9 | y9 | A, B, C | 5.6 | 5R6 | U0 | A, B, C, D | 43 | 430 | R1 | F, G, J, K, M |
| 1.0 | 1R0 | A0 | A, B, C, D | 6.2 | 6R2 | V0 | A, B, C, D | 47 | 470 | S1 | F, G, J, K, M |
| 1.1 | 1R1 | B0 | A, B, C, D | 6.8 | 6R8 | W0 | B, C, D, K | 51 | 510 | T1 | F, G, J, K, M |
| 1.2 | 1R2 | C0 | A, B, C, D | 7.5 | 7R5 | X0 | B, C, D, K | 56 | 560 | U1 | F, G, J, K, M |
| 1.3 | 1R3 | D0 | A, B, C, D | 8.2 | 8R2 | Y0 | B, C, D, K | 62 | 620 | V1 | F, G, J, K, M |
| 1.5 | 1R5 | E0 | A, B, C, D | 9.1 | 9R1 | Z0 | B, C, D, K | 68 | 680 | W1 | F, G, J, K, M |
| 1.6 | 1R6 | F0 | A, B, C, D | 10 | 100 | A1 | F, G, J, K, M | 75 | 750 | X1 | F, G, J, K, M |
| 1.8 | 1R8 | G0 | A, B, C, D | 11 | 110 | B1 | F, G, J, K, M | 82 | 820 | Y1 | F, G, J, K, M |
| 2.0 | 2R0 | H0 | A, B, C, D | 12 | 120 | C1 | F, G, J, K, M | 91 | 910 | Z1 | F, G, J, K, M |
| 2.2 | 2R2 | J0 | A, B, C, D | 15 | 150 | E1 | F, G, J, K, M | 100 | 101 | A2 | F, G, J, K, M |
| 2.4 | 2R4 | K0 | A, B, C, D | 18 | 180 | G1 | F, G, J, K, M | | | | |

*Non-standard values and custom tolerances are available upon request.

## ATC Part Number Code




TOLERANCE CODE TABLE

| Code | A | B | C | D | F | G | J | K | M |
|---|---|---|---|---|---|---|---|---|---|
| Tol. | ±0.05pF | ±0.1 pF | ±0.25 pF | ±0.5 pF | ±1% | ±2% | ±5% | ±10% | ±20% |

*4,000 pieces on 7" reel and 500 pieces on prototype reel. Consult ATC for other options.

The above part number refers to a 600S Series (case size S) 0.2 pF capacitor, B tolerance (±0.1pF), 250 WVDC, with T termination (Tin Plated over Nickel Barrier, RoHS Compliant), Laser Marking and Tape and Reel packaging.

**Marking is optional.

ATC accepts orders for our parts using designations *with* or *without* the "ATC" prefix. Both methods of defining the part number are equivalent, i.e., part numbers referenced with the "ATC" prefix are interchangeable to parts referenced without the "ATC" prefix. Customers are free to use either in specifying or procuring parts from American Technical Ceramics.

For additional information and catalogs contact your ATC representative or call direct at (631) 622-4700.

*Consult factory for 500 piece reels for prototyping.

Consult factory for additional performance data.

AMERICAN TECHNICAL CERAMICS

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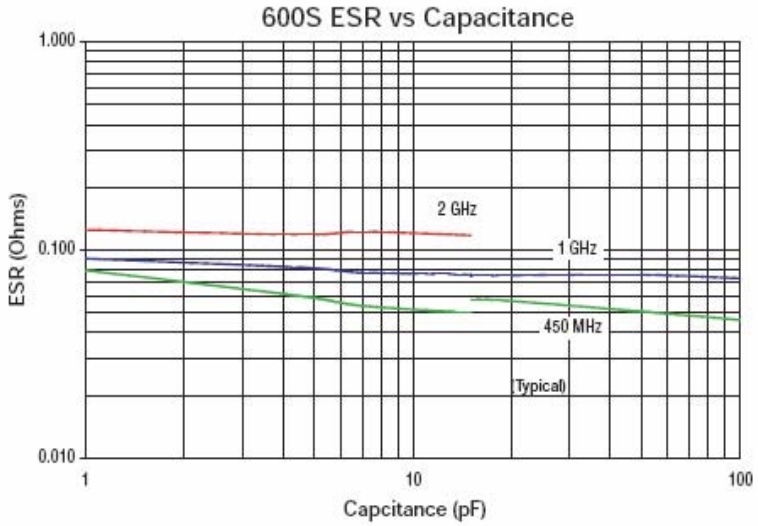
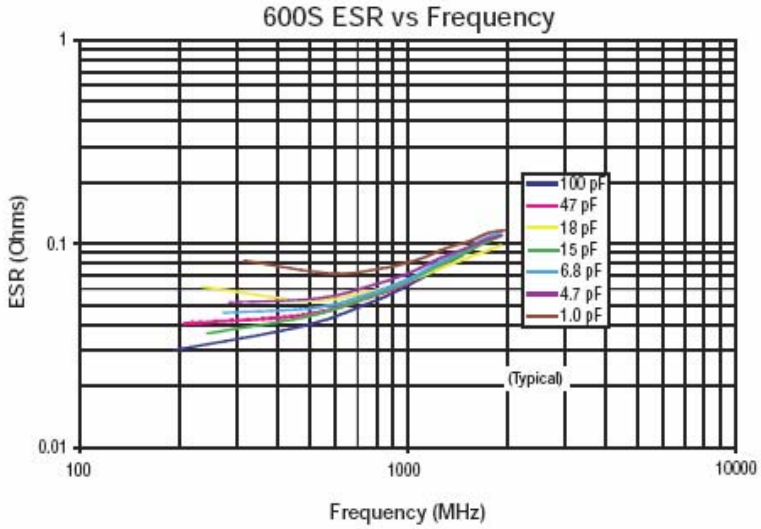
ATC Europe +46 8 6800410 sales@atceramics-europe.com

ATC Asia 86-755-8366-4318 sales@atceramics-asia.com

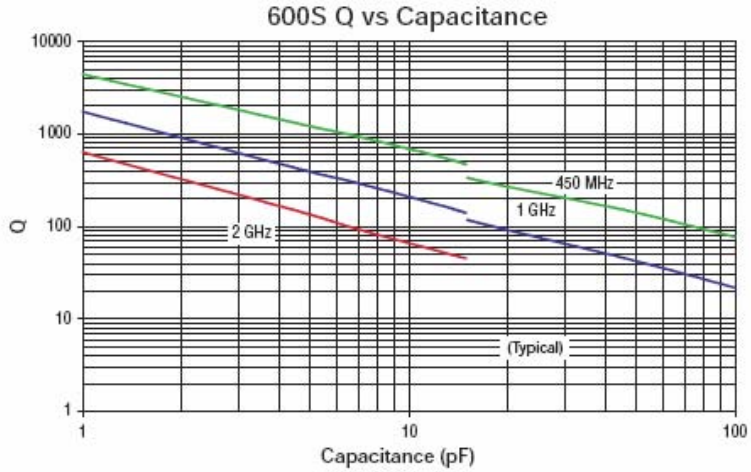
## ATC 600S Series Ultra-Low ESR, High Q NPO RF & Microwave Capacitors

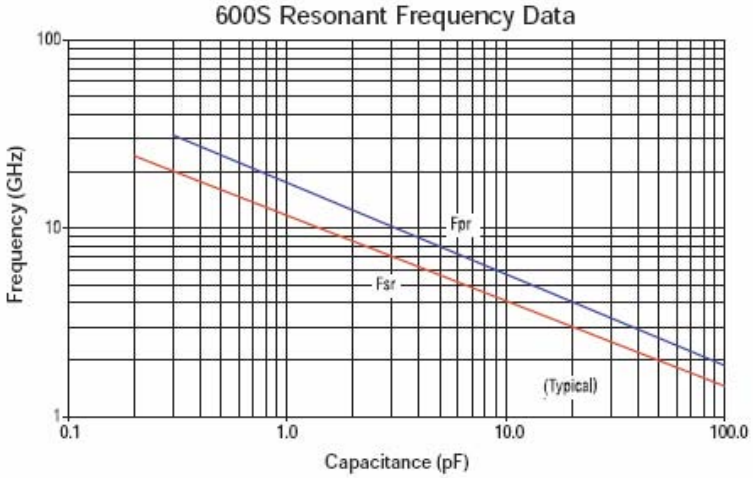
### Typical Performance Data



## ATC 600S Series Ultra-Low ESR, High Q NPO RF & Microwave Capacitors



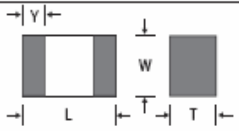




**ATC 600 Series Data Sheet Test Condition Description**

Capacitors horizontally mounted on 13.3-mil thick Rogers RO4350® softboard, 29-mil wide, 1/2 oz. Cu traces.
**FSR** = lowest frequency at which S11 response, referenced at capacitor edge, crosses real axis on Smith Chart.
**FPR** = lowest frequency at which there is a notch in S21 magnitude response.

# ATC 600S Series Ultra-Low ESR, NPO RF & Microwave Capacitors

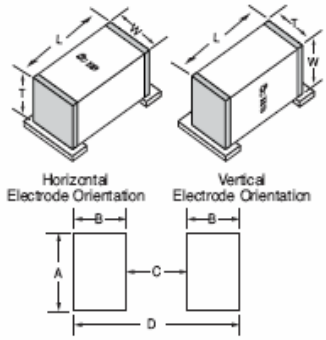
## Outline Dimensions




| | | |
|---|---|---|
| S (0603) | L: .063 ± .006 (1.60 ± .15)<br>W: .032 ± .006 (.81 ± .15) | T: .035 max. (0.89 max.)<br>Y: .014 ± .006 (0.36 ± 0.15) |

*Inches (mm)*

## Suggested Mounting Pad Dimensions




Case Sizes L, S and F

| Case Size | A Min. | B Min. | C Min. | D Min. |
|---|---|---|---|---|
| 0402 (1005) | .0275 (0.70) | .0354 (0.90) | .0157 (0.40) | .0866 (2.20) |
| 0603 (1608) | .0393 (1.00) | .0433 (1.10) | .0236 (0.60) | .110 (2.80) |
| 0805 (2012) | .0590 (1.50) | .0512 (1.30) | .0236 (0.60) | .1259 (3.20) |

Inches (mm)

**Design Kits** Each Kit contains a selection of standard capacitor values for circuit prototyping.

| Kit # | Item # | Description | Cap. Value Range (pF) | Cap. Values (pF) | Tol. (pF) | Price |
|---|---|---|---|---|---|---|
| Kit 25T | DK0025T | 600S Series Ultra-low ESR, High Q Microwave Capacitors<br>16 different values, 15 pcs. min. per value | 0.1 to 2.0 | 0.1, 0.2, 0.3, 0.4, 0.5, 0.6 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.5 | ±0.1 | $90.00 |
| | | | | 1.6, 1.8, 2.0 | ±0.25 | |
| Kit 26T | DK0026T | 600S Series Ultra-low ESR, High Q Microwave Capacitors<br>16 different values, 15 pcs. min. per value | 1.0 to 10 | 1.0, 1.2 1.5, 1.8, 2.0, 2.2, 2.4, 2.7, 3.0, 3.3 | ±0.1 | $90.00 |
| | | | | 3.9, 4.7, 5.6, 6.8, 8.2 | ±0.25 | |
| | | | | 10 | ±5% | |
| Kit 27T | DK0027T | 600S Series Ultra-low ESR, High Q Microwave Capacitors<br>16 different values, 15 pcs. min. per value | 10 to 100 | 10, 12, 15, 18, 20, 22, 24, 27, 30, 33, 39, 47, 56, 68, 82, 100 | ±5% | $90.00 |

For Online Kit Orders, Catalog & Application Notes, **Visit: www.atceramics.com**